MF1323-04

S1D10605 Series

Rev.1.0a

Contents

1. DESCRIPTION

The S1D10605 Series is a series of single-chip dot matrix liquid crystal display drivers that can be connected directly to a microprocessor bus. 8-bit parallel or serial display data sent from the microprocessor is stored in the internal display data RAM and the chip generates a liquid crystal drive signal independent of the microprocessor. Because the chips in the S1D10605 Series contain 65 × 132 bits of display data RAM and there is a 1-to-1 correspondence between the liquid crystal panel pixels and the internal RAM bits, these chips enable displays with a high degree of freedom.
The S1D10606 Series chips contain 65 common output circuits and 132 segment output circuits, so that a single chip can drive a 65 × 132 dot display (capable of displaying 8 columns × 4 rows of a 16 × 16 dot kanji font). The S1D10607 Series chips contain 33 common output circuits and 132 segment output circuits, so that a single chip can drive 33 × 132 dot display (capable of displaying 8 columns × 2 rows of 16 × 16 dot kanji fonts). Thanks to the built-in 55 common output circuits and 132 segment output circuits, the S1D10608 Series is capable of displaying 55 × 132 dots (11 columns × 4 lines using 11 × 12 dots Kanji font) with a single chip.
The S1D10609 Series chips contain 53 common output circuits and 132 segment output circuits, so that a single chip can drive 53 × 132 dot display (capable of displaying 11 columns × 4 rows of 11 × 12 dot kanji fonts). Moreover, the capacity of the display can be extended through the use of master/slave structures between chips.
The chips are able to minimize power consumption because no external operating clock is necessary for the display data RAM read/write operation. Furthermore, because each chip is equipped internally with a low-power liquid crystal driver power supply, resistors for liquid crystal driver power voltage adjustment and a display clock CR oscillator circuit, the S1D10605 Series chips can be used to create the lowest power display system with the fewest components for high-performance portable devices.

2. FEATURES

- Direct display of RAM data through the display data RAM.
  RAM bit data: "1" Display on
  "0" Display off
  (during normal display)
- RAM capacity
  65 × 132 = 8580 bits
- Display driver circuits
  S1D10605*****: 65 common output and 132 segment outputs
  S1D10606*****: 49 common output and 132 segment outputs
  S1D10607*****: 33 common outputs and 132 segment outputs
  S1D10608*****: 55 common outputs and 132 segment outputs
  S1D10609*****: 53 common outputs and 132 segment outputs
- High-speed 8-bit MPU interface (The chip can be connected directly to the both the 80x86 series MPUs and the 6800 series MPUs)
  /Serial interfaces are supported.
- Abundant command functions
  Display data Read/Write, display ON/OFF, Normal/Reverse display mode, page address set, display start line set, column address set, status read, display all points ON/OFF, LCD bias set, electronic volume, read/modify/write, segment driver direction select, power saver, static indicator, common output status select, V5 voltage regulation internal resistor ratio set.
- Static drive circuit equipped internally for indicators. (1 system, with variable flashing speed.)
- Low-power liquid crystal display power supply circuit equipped internally.
  Booster circuit (with Boost ratios of Double/Triple/Quad, where the step-up voltage reference power supply can be input externally)
  High-accuracy voltage adjustment circuit (Thermal gradient –0.05%/°C)
  V_5 voltage regulator resistors equipped internally, V_1 to V_4 voltage divider resistors equipped internally, electronic volume function equipped internally, voltage follower.
- CR oscillator circuit equipped internally (external clock can also be input)
- Extremely low power consumption
  Operating power when the built-in power supply is used (an example)

S1D10605D00B*	TBD μA ($V_{DD} – V_{SS} = V_{DD} – V_{SS2}$ = 3.0 V, Quad voltage, $V_5 – V_{DD}$ = – 11.0 V)
S1D10606D00B*	TBD μA ($V_{DD} – V_{SS} = V_{DD} – V_{SS2}$ = 3.0 V, Triple voltage, $V_5 – V_{DD}$ = – 8.0 V)
S1D10607D00B*	TBD μA ($V_{DD} – V_{SS} = V_{DD} – V_{SS2}$ = 3.0 V, Triple voltage, $V_5 – V_{DD}$ = – 8.0 V)
S1D10608D00B* /S1D10609D00B*	TBD μA ($V_{DD} – V_{SS} = V_{DD} – V_{SS2}$ = 3.0 V, Triple voltage, $V_5 – V_{DD}$ = – 8.0 V)

  Conditions: When all displays are in white and the normal mode is selected (see page 60 *12 for details of the conditions).
- Power supply
  Operable on the low 1.8 voltage
  Logic power supply $V_{DD} – V_{SS}$ = 1.8 V to –3.6 V
  Boost reference voltage: $V_{DD} – V_{SS2}$ = 1.8 V to –4.0 V
  Liquid crystal drive power supply: $V_{DD} – V_5$ = –4.5 V to –14.0 V
- Wide range of operating temperatures: –40 to 85°C
- CMOS process
- Shipping forms include bare chip and TCP.
- These chips not designed for resistance to light or resistance to radiation.

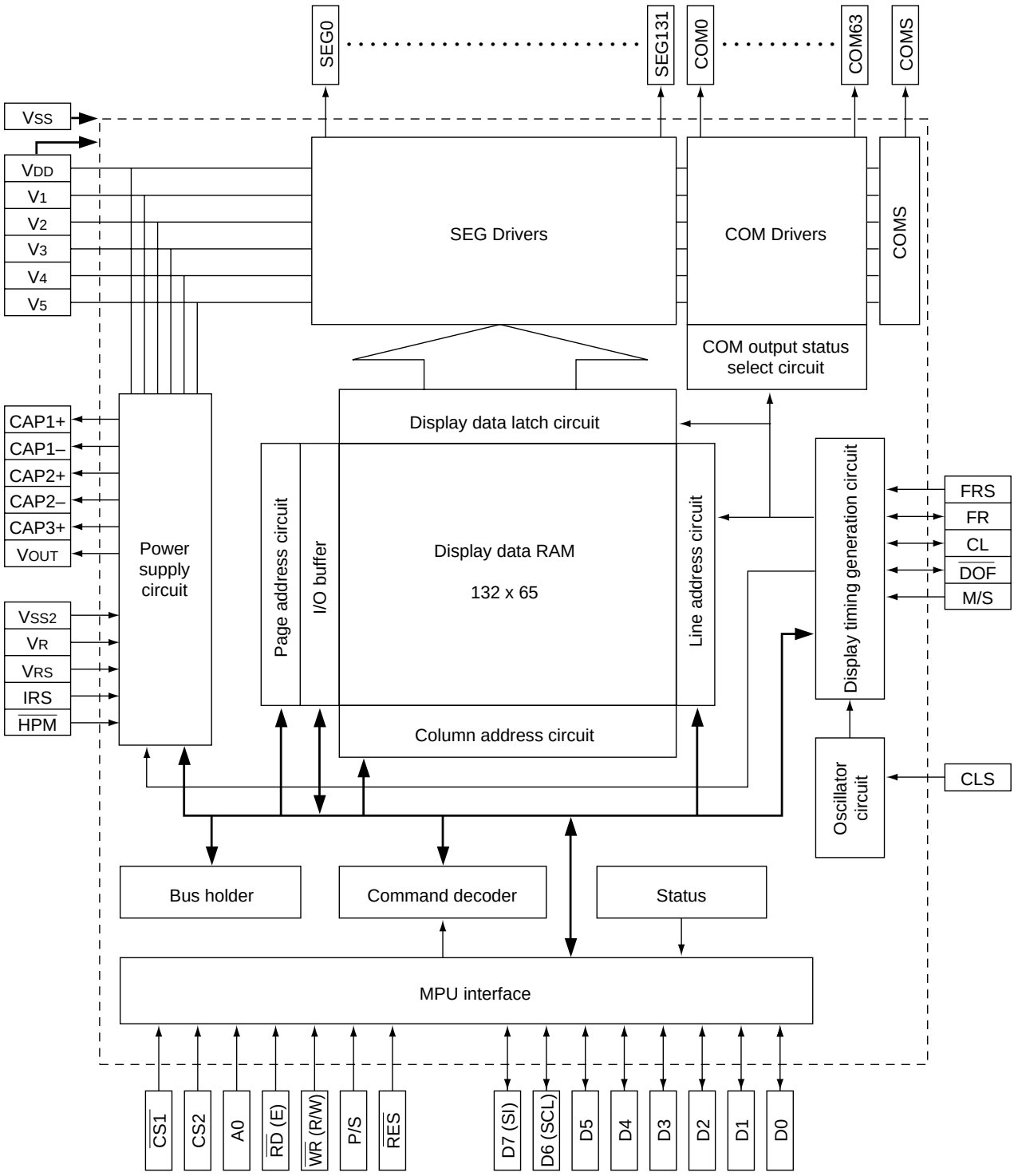
Series Specifications

Product Name	Duty	Bias	SED Dr	COM Dr	VREG Temperature Gradient	Shipping Forms	Chip Thickness
S1D10605D00B*	1/65	1/9, 1/7	132	65	–0.05%/°C	Bare Chip	625 µm
S1D10605T00**						TCP	—
** S1D10606D00B*	1/49	1/8, 1/6		49		Bare Chip	625 µm
** S1D10606T00**						TCP	—
** S1D10607D00B*	1/33	1/6, 1/5		33		Bare Chip	625 µm
** S1D10607T00**						TCP	—
** S1D10608D00B*	1/55	1/8, 1/6		55		Bare Chip	625 µm
** S1D10609D00B*	1/53	1/8, 1/6		53		Bare Chip	625 µm
** S1D10609T00**						TCP	—

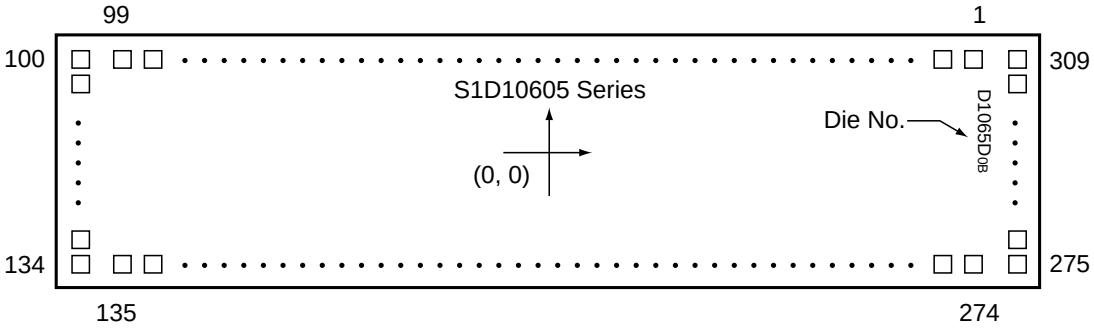
* * : Being Planned.

3. BLOCK DIAGRAM

Example: S1D10605***



4. PAD LAYOUT



Item		Size X Y	Unit
Chip Size		7.93 × 2.25	mm
Chip Thickness		0.625	
Bump Pitch		50 (Min.)	μm
Bump Size	PAD No. 1 to 24	55 × 76	
	PAD No. 25 to 82	45 × 76	
	PAD No. 83 to 99	55 × 76	
	PAD No. 100 to 134	136 × 33	
	PAD No. 135 to 274	33 × 126	
	PAD No. 275 to 309	136 × 33	
Bump Height		17 (Typ.)	
Alignment Mark Left Upper ◎	Alignment Coordinates	–3590 × 980	
	Outside Diameter • Inside Diameter	78 • 33	
Alignment Mark Left Lower ◎	Alignment Coordinates	–3690 × –940	
	Outside Diameter • Inside Diameter	78 • 33	
Alignment Mark Right Upper ○	Alignment Coordinates	3635 × 980	
	Outside Diameter	78	
Alignment Mark Right Lower ○	Alignment Coordinates	3585 × –940	
	Outside Diameter	78	

5. PAD CENTER COORDINATES

Units: μm

PAD No.	PIN Name					X	Y	X BUMP Size	Y BUMP Size
	S1D10605	S1D10606	S1D10607	S1D10608	S1D10609				
1	DUMMY1	DUMMY1	DUMMY1	DUMMY1	DUMMY1	3443	983	55	76
2	FRS	FRS	FRS	FRS	FRS	3360			
3	FR	FR	FR	FR	FR	3277			
4	CL	CL	CL	CL	CL	3194			
5	$\overline{DOF}$	$\overline{DOF}$	$\overline{DOF}$	$\overline{DOF}$	$\overline{DOF}$	3111			
6	TEST0	TEST0	TEST0	TEST0	TEST0	3029			
7	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	2946			
8	$\overline{CS1}$	$\overline{CS1}$	$\overline{CS1}$	$\overline{CS1}$	$\overline{CS1}$	2863			
9	CS2	CS2	CS2	CS2	CS2	2780			
10	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	2697			
11	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$	2615			
12	A0	A0	A0	A0	A0	2532			
13	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	2449			
14	$\overline{WR}$,R/$\overline{W}$	$\overline{WR}$,R/$\overline{W}$	$\overline{WR}$,R/$\overline{W}$	$\overline{WR}$,R/$\overline{W}$	$\overline{WR}$,R/$\overline{W}$	2366			
15	$\overline{RD}$,E	$\overline{RD}$,E	$\overline{RD}$,E	$\overline{RD}$,E	$\overline{RD}$,E	2283			
16	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	2201			
17	D0	D0	D0	D0	D0	2118			
18	D1	D1	D1	D1	D1	2035			
19	D2	D2	D2	D2	D2	1952			
20	D3	D3	D3	D3	D3	1869			
21	D4	D4	D4	D4	D4	1787			
22	D5	D5	D5	D5	D5	1704			
23	D6,SCL	D6,SCL	D6,SCL	D6,SCL	D6,SCL	1621			
24	D7,SI	D7,SI	D7,SI	D7,SI	D7,SI	1538		▼	
25	DUMMY2	DUMMY2	DUMMY2	DUMMY2	DUMMY2	1469		45	
26	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	1408			
27	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	1346			
28	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	1284			
29	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	1223			
30	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	1161			
31	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	1099			
32	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	1038			
33	V_{SS2}	V_{SS2}	V_{SS2}	V_{SS2}	V_{SS2}	976			
34	V_{SS2}	V_{SS2}	V_{SS2}	V_{SS2}	V_{SS2}	914			
35	V_{SS2}	V_{SS2}	V_{SS2}	V_{SS2}	V_{SS2}	853			
36	V_{SS2}	V_{SS2}	V_{SS2}	V_{SS2}	V_{SS2}	791			
37	DUMMY3	DUMMY3	DUMMY3	DUMMY3	DUMMY3	729			
38	V_{OUT}	V_{OUT}	V_{OUT}	V_{OUT}	V_{OUT}	668			
39	V_{OUT}	V_{OUT}	V_{OUT}	V_{OUT}	V_{OUT}	606			
40	CAP3–	CAP3–	CAP3–	CAP3–	CAP3–	544			
41	CAP3–	CAP3–	CAP3–	CAP3–	CAP3–	483			
42	DUMMY4	DUMMY4	DUMMY4	DUMMY4	DUMMY4	421			
43	CAP1+	CAP1+	CAP1+	CAP1+	CAP1+	359			
44	CAP1+	CAP1+	CAP1+	CAP1+	CAP1+	298			
45	CAP1–	CAP1–	CAP1–	CAP1–	CAP1–	236			
46	CAP1–	CAP1–	CAP1–	CAP1–	CAP1–	175			
47	CAP2–	CAP2–	CAP2–	CAP2–	CAP2–	113			
48	CAP2–	CAP2–	CAP2–	CAP2–	CAP2–	51			
49	CAP2+	CAP2+	CAP2+	CAP2+	CAP2+	–10			
50	CAP2+	CAP2+	CAP2+	CAP2+	CAP2+	–72			
51	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	–134			
52	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	–195			
53	V_{RS}	V_{RS}	V_{RS}	V_{RS}	V_{RS}	–257			
54	V_{RS}	V_{RS}	V_{RS}	V_{RS}	V_{RS}	–319	▼	▼	▼

Unit : μm

PAD No.	PIN Name					X	Y	X BUMP Size	Y BUMP Size
	S1D10605	S1D10606	S1D10607	S1D10608	S1D10609				
55	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	–380	983	45	76
56	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	–442			
57	V_1	V_1	V_1	V_1	V_1	–504			
58	V_1	V_1	V_1	V_1	V_1	–565			
59	V_2	V_2	V_2	V_2	V_2	–627			
60	V_2	V_2	V_2	V_2	V_2	–689			
61	DUMMY5	DUMMY5	DUMMY5	DUMMY5	DUMMY5	–750			
62	V_3	V_3	V_3	V_3	V_3	–812			
63	V_3	V_3	V_3	V_3	V_3	–874			
64	V_4	V_4	V_4	V_4	V_4	–935			
65	V_4	V_4	V_4	V_4	V_4	–997			
66	V_5	V_5	V_5	V_5	V_5	–1058			
67	V_5	V_5	V_5	V_5	V_5	–1120			
68	DUMMY6	DUMMY6	DUMMY6	DUMMY6	DUMMY6	–1182			
69	V_R	V_R	V_R	V_R	V_R	–1243			
70	V_R	V_R	V_R	V_R	V_R	–1305			
71	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	–1367			
72	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	–1428			
73	TEST1	TEST1	TEST1	TEST1	TEST1	–1490			
74	TEST1	TEST1	TEST1	TEST1	TEST1	–1552			
75	TEST2	TEST2	TEST2	TEST2	TEST2	–1613			
76	TEST2	TEST2	TEST2	TEST2	TEST2	–1675			
77	DUMMY7	DUMMY7	DUMMY7	DUMMY7	DUMMY7	–1737			
78	TEST3	TEST3	TEST3	TEST3	TEST3	–1798			
79	TEST3	TEST3	TEST3	TEST3	TEST3	–1860			
80	TEST4	TEST4	TEST4	TEST4	TEST4	–1922			
81	TEST4	TEST4	TEST4	TEST4	TEST4	–1983			
82	DUMMY8	DUMMY8	DUMMY8	DUMMY8	DUMMY8	–2045		▼	
83	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	–2118		55	
84	M/S	M/S	M/S	M/S	M/S	–2201			
85	CLS	CLS	CLS	CLS	CLS	–2283			
86	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	–2366			
87	C86	C86	C86	C86	C86	–2449			
88	P/S	P/S	P/S	P/S	P/S	–2532			
89	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	–2615			
90	$\overline{HPM}$	$\overline{HPM}$	$\overline{HPM}$	$\overline{HPM}$	$\overline{HPM}$	–2697			
91	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	–2780			
92	IRS	IRS	IRS	IRS	IRS	–2863			
93	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	–2946			
94	TEST5	TEST5	TEST5	TEST5	TEST5	–3029			
95	TEST6	TEST6	TEST6	TEST6	TEST6	–3111			
96	TEST7	TEST7	TEST7	TEST7	TEST7	–3194			
97	TEST8	TEST8	TEST8	TEST8	TEST8	–3277			
98	TEST9	TEST9	TEST9	TEST9	TEST9	–3360			
99	TESTA	TESTA	TESTA	TESTA	TESTA	–3443	▼	▼	▼
100	DUMMY9	DUMMY9	DUMMY9	DUMMY9	DUMMY9	–3794	865	136	33
101	COM31	DUMMY10	COM15	DUMMY10	DUMMY10		815		
102	COM30	DUMMY11	COM15	COM26	COM25		765		
103	COM29	COM23	COM14	DUMMY11	DUMMY11		715		
104	COM28	DUMY12	COM14	COM25	COM24		665		
105	COM27	COM22	COM13	COM24	DUMMY12		615		
106	COM26	DUMMY13	COM13	COM23	COM23		565		
107	COM25	COM21	COM12	COM22	COM22		515		
108	COM24	COM20	COM12	COM21	COM21	▼	465	▼	▼

Units : μm

PAD No.	PIN Name					X	Y	X BUMP Size	Y BUMP Size
	S1D10605	S1D10606	S1D10607	S1D10608	S1D10609				
109	COM23	COM19	COM11	COM20	COM20	–3794	415	136	33
110	COM22	COM18	COM11	COM19	COM19		365		
111	COM21	COM17	COM10	COM18	COM18		314		
112	COM20	COM16	COM10	COM17	COM17		264		
113	COM19	COM15	COM9	COM16	COM16		214		
114	COM18	COM14	COM9	COM15	COM15		164		
115	COM17	COM13	COM8	COM14	COM14		114		
116	COM16	COM12	COM8	COM13	COM13		64		
117	COM15	COM11	COM7	COM12	COM12		14		
118	COM14	COM10	COM7	COM11	COM11		–36		
119	COM13	COM9	COM6	COM10	COM10		–86		
120	COM12	COM8	COM6	COM9	COM9		–136		
121	COM11	COM7	COM5	COM8	COM8		–186		
122	COM10	COM6	COM5	COM7	COM7		–236		
123	COM9	COM5	COM4	COM6	COM6		–286		
124	COM8	COM4	COM4	COM5	COM5		–336		
125	COM7	COM3	COM3	COM4	COM4		–386		
126	COM6	COM2	COM3	COM3	COM3		–436		
127	COM5	COM1	COM2	COM2	COM2		–486		
128	COM4	DUMMY14	COM2	COM1	COM1		–536		
129	COM3	COM0	COM1	DUMMY12	DUMMY13		–586		
130	COM2	DUMMY15	COM1	COM0	COM0		–636		
131	COM1	COMS	COM0	DUMMY13	DUMMY14		–686		
132	COM0	DUMMY16	COM0	COMS	COMS		–736		
133	COMS	DUMMY17	COMS	DUMMY14	DUMMY15		–786		
134	DUMMY10	DUMMY18	DUMMY10	DUMMY15	DUMMY16	▼	–836	▼	▼
135	DUMMY11	DUMMY19	DUMMY11	DUMMY16	DUMMY17	–3478	–958	33	126
136	DUMMY12	DUMMY20	DUMMY12	DUMMY17	DUMMY18	–3428			
137	DUMMY13	DUMMY21	DUMMY13	DUMMY18	DUMMY19	–3378			
138	DUMMY14	DUMMY22	DUMMY14	DUMMY19	DUMMY20	–3328			
139	SEG0	SEG0	SEG0	SEG0	SEG0	–3278			
140	SEG1	SEG1	SEG1	SEG1	SEG1	–3228			
141	SEG2	SEG2	SEG2	SEG2	SEG2	–3178			
142	SEG3	SEG3	SEG3	SEG3	SEG3	–3128			
143	SEG4	SEG4	SEG4	SEG4	SEG4	–3077			
144	SEG5	SEG5	SEG5	SEG5	SEG5	–3027			
145	SEG6	SEG6	SEG6	SEG6	SEG6	–2977			
146	SEG7	SEG7	SEG7	SEG7	SEG7	–2927			
147	SEG8	SEG8	SEG8	SEG8	SEG8	–2877			
148	SEG9	SEG9	SEG9	SEG9	SEG9	–2827			
149	SEG10	SEG10	SEG10	SEG10	SEG10	–2777			
150	SEG11	SEG11	SEG11	SEG11	SEG11	–2727			
151	SEG12	SEG12	SEG12	SEG12	SEG12	–2677			
152	SEG13	SEG13	SEG13	SEG13	SEG13	–2627			
153	SEG14	SEG14	SEG14	SEG14	SEG14	–2577			
154	SEG15	SEG15	SEG15	SEG15	SEG15	–2527			
155	SEG16	SEG16	SEG16	SEG16	SEG16	–2477			
156	SEG17	SEG17	SEG17	SEG17	SEG17	–2427			
157	SEG18	SEG18	SEG18	SEG18	SEG18	–2377			
158	SEG19	SEG19	SEG19	SEG19	SEG19	–2327			
159	SEG20	SEG20	SEG20	SEG20	SEG20	–2277			
160	SEG21	SEG21	SEG21	SEG21	SEG21	–2227			
161	SEG22	SEG22	SEG22	SEG22	SEG22	–2177			
162	SEG23	SEG23	SEG23	SEG23	SEG23	–2127	▼	▼	▼

Units : μm

PAD No.	PIN Name					X	Y	X BUMP Size	Y BUMP Size
	S1D10605	S1D10606	S1D10607	S1D10608	S1D10609				
163	SEG24	SEG24	SEG24	SEG24	SEG24	–2077	–958	33	126
164	SEG25	SEG25	SEG25	SEG25	SEG25	–2027			
165	SEG26	SEG26	SEG26	SEG26	SEG26	–1977			
166	SEG27	SEG27	SEG27	SEG27	SEG27	–1927			
167	SEG28	SEG28	SEG28	SEG28	SEG28	–1877			
168	SEG29	SEG29	SEG29	SEG29	SEG29	–1826			
169	SEG30	SEG30	SEG30	SEG30	SEG30	–1776			
170	SEG31	SEG31	SEG31	SEG31	SEG31	–1726			
171	SEG32	SEG32	SEG32	SEG32	SEG32	–1676			
172	SEG33	SEG33	SEG33	SEG33	SEG33	–1626			
173	SEG34	SEG34	SEG34	SEG34	SEG34	–1576			
174	SEG35	SEG35	SEG35	SEG35	SEG35	–1526			
175	SEG36	SEG36	SEG36	SEG36	SEG36	–1476			
176	SEG37	SEG37	SEG37	SEG37	SEG37	–1426			
177	SEG38	SEG38	SEG38	SEG38	SEG38	–1376			
178	SEG39	SEG39	SEG39	SEG39	SEG39	–1326			
179	SEG40	SEG40	SEG40	SEG40	SEG40	–1276			
180	SEG41	SEG41	SEG41	SEG41	SEG41	–1226			
181	SEG42	SEG42	SEG42	SEG42	SEG42	–1176			
182	SEG43	SEG43	SEG43	SEG43	SEG43	–1126			
183	SEG44	SEG44	SEG44	SEG44	SEG44	–1076			
184	SEG45	SEG45	SEG45	SEG45	SEG45	–1026			
185	SEG46	SEG46	SEG46	SEG46	SEG46	–976			
186	SEG47	SEG47	SEG47	SEG47	SEG47	–926			
187	SEG48	SEG48	SEG48	SEG48	SEG48	–876			
188	SEG49	SEG49	SEG49	SEG49	SEG49	–826			
189	SEG50	SEG50	SEG50	SEG50	SEG50	–776			
190	SEG51	SEG51	SEG51	SEG51	SEG51	–726			
191	SEG52	SEG52	SEG52	SEG52	SEG52	–676			
192	SEG53	SEG53	SEG53	SEG53	SEG53	–626			
193	SEG54	SEG54	SEG54	SEG54	SEG54	–575			
194	SEG55	SEG55	SEG55	SEG55	SEG55	–525			
195	SEG56	SEG56	SEG56	SEG56	SEG56	–475			
196	SEG57	SEG57	SEG57	SEG57	SEG57	–425			
197	SEG58	SEG58	SEG58	SEG58	SEG58	–375			
198	SEG59	SEG59	SEG59	SEG59	SEG59	–325			
199	SEG60	SEG60	SEG60	SEG60	SEG60	–275			
200	SEG61	SEG61	SEG61	SEG61	SEG61	–225			
201	SEG62	SEG62	SEG62	SEG62	SEG62	–175			
202	SEG63	SEG63	SEG63	SEG63	SEG63	–125			
203	SEG64	SEG64	SEG64	SEG64	SEG64	–75			
204	SEG65	SEG65	SEG65	SEG65	SEG65	–25			
205	SEG66	SEG66	SEG66	SEG66	SEG66	25			
206	SEG67	SEG67	SEG67	SEG67	SEG67	75			
207	SEG68	SEG68	SEG68	SEG68	SEG68	125			
208	SEG69	SEG69	SEG69	SEG69	SEG69	175			
209	SEG70	SEG70	SEG70	SEG70	SEG70	225			
210	SEG71	SEG71	SEG71	SEG71	SEG71	275			
211	SEG72	SEG72	SEG72	SEG72	SEG72	325			
212	SEG73	SEG73	SEG73	SEG73	SEG73	375			
213	SEG74	SEG74	SEG74	SEG74	SEG74	425			
214	SEG75	SEG75	SEG75	SEG75	SEG75	475			
215	SEG76	SEG76	SEG76	SEG76	SEG76	525			
216	SEG77	SEG77	SEG77	SEG77	SEG77	575	▼	▼	▼

Units : μm

PAD No.	PIN Name					X	Y	X BUMP Size	Y BUMP Size
	S1D10605	S1D10606	S1D10607	S1D10608	S1D10609				
217	SEG78	SEG78	SEG78	SEG78	SEG78	626	–958	33	126
218	SEG79	SEG79	SEG79	SEG79	SEG79	676			
219	SEG80	SEG80	SEG80	SEG80	SEG80	726			
220	SEG81	SEG81	SEG81	SEG81	SEG81	776			
221	SEG82	SEG82	SEG82	SEG82	SEG82	826			
222	SEG83	SEG83	SEG83	SEG83	SEG83	876			
223	SEG84	SEG84	SEG84	SEG84	SEG84	926			
224	SEG85	SEG85	SEG85	SEG85	SEG85	976			
225	SEG86	SEG86	SEG86	SEG86	SEG86	1026			
226	SEG87	SEG87	SEG87	SEG87	SEG87	1076			
227	SEG88	SEG88	SEG88	SEG88	SEG88	1126			
228	SEG89	SEG89	SEG89	SEG89	SEG89	1176			
229	SEG90	SEG90	SEG90	SEG90	SEG90	1226			
230	SEG91	SEG91	SEG91	SEG91	SEG91	1276			
231	SEG92	SEG92	SEG92	SEG92	SEG92	1326			
232	SEG93	SEG93	SEG93	SEG93	SEG93	1376			
233	SEG94	SEG94	SEG94	SEG94	SEG94	1426			
234	SEG95	SEG95	SEG95	SEG95	SEG95	1476			
235	SEG96	SEG96	SEG96	SEG96	SEG96	1526			
236	SEG97	SEG97	SEG97	SEG97	SEG97	1576			
237	SEG98	SEG98	SEG98	SEG98	SEG98	1626			
238	SEG99	SEG99	SEG99	SEG99	SEG99	1676			
239	SEG100	SEG100	SEG100	SEG100	SEG100	1726			
240	SEG101	SEG101	SEG101	SEG101	SEG101	1776			
241	SEG102	SEG102	SEG102	SEG102	SEG102	1826			
242	SEG103	SEG103	SEG103	SEG103	SEG103	1877			
243	SEG104	SEG104	SEG104	SEG104	SEG104	1927			
244	SEG105	SEG105	SEG105	SEG105	SEG105	1977			
245	SEG106	SEG106	SEG106	SEG106	SEG106	2027			
246	SEG107	SEG107	SEG107	SEG107	SEG107	2077			
247	SEG108	SEG108	SEG108	SEG108	SEG108	2127			
248	SEG109	SEG109	SEG109	SEG109	SEG109	2177			
249	SEG110	SEG110	SEG110	SEG110	SEG110	2227			
250	SEG111	SEG111	SEG111	SEG111	SEG111	2277			
251	SEG112	SEG112	SEG112	SEG112	SEG112	2327			
252	SEG113	SEG113	SEG113	SEG113	SEG113	2377			
253	SEG114	SEG114	SEG114	SEG114	SEG114	2427			
254	SEG115	SEG115	SEG115	SEG115	SEG115	2477			
255	SEG116	SEG116	SEG116	SEG116	SEG116	2527			
256	SEG117	SEG117	SEG117	SEG117	SEG117	2577			
257	SEG118	SEG118	SEG118	SEG118	SEG118	2627			
258	SEG119	SEG119	SEG119	SEG119	SEG119	2677			
259	SEG120	SEG120	SEG120	SEG120	SEG120	2727			
260	SEG121	SEG121	SEG121	SEG121	SEG121	2777			
261	SEG122	SEG122	SEG122	SEG122	SEG122	2827			
262	SEG123	SEG123	SEG123	SEG123	SEG123	2877			
263	SEG124	SEG124	SEG124	SEG124	SEG124	2927			
264	SEG125	SEG125	SEG125	SEG125	SEG125	2977			
265	SEG126	SEG126	SEG126	SEG126	SEG126	3027			
266	SEG127	SEG127	SEG127	SEG127	SEG127	3077			
267	SEG128	SEG128	SEG128	SEG128	SEG128	3128			
268	SEG129	SEG129	SEG129	SEG129	SEG129	3178			
269	SEG130	SEG130	SEG130	SEG130	SEG130	3228			
270	SEG131	SEG131	SEG131	SEG131	SEG131	3278	▼	▼	▼

Units : μm

PAD No.	PIN Name					X	Y	X BUMP Size	Y BUMP Size
	S1D10605	S1D10606	S1D10607	S1D10608	S1D10609				
271	DUMMY15	DUMMY23	DUMMY15	DUMMY20	DUMMY21	3328	–958	33	126
272	DUMMY16	DUMMY24	DUMMY16	DUMMY21	DUMMY22	3378			
273	DUMMY17	DUMMY25	DUMMY17	DUMMY22	DUMMY23	3428			
274	DUMMY18	DUMMY26	DUMMY18	DUMMY23	DUMMY24	3478			
275	DUMMY19	DUMMY27	DUMMY19	DUMMY24	DUMMY25	3794	–836	136	33
276	COM32	DUMMY28	COM16	DUMMY25	DUMMY26		–786		
277	COM33	DUMMY29	COM16	COM27	COM26		–736		
278	COM34	COM24	COM17	DUMMY26	DUMMY27		–686		
279	COM35	DUMMY30	COM17	COM28	COM27		–636		
280	COM36	COM25	COM18	DUMMY27	DUMMY28		–586		
281	COM37	DUMMY31	COM18	COM29	COM28		–536		
282	COM38	COM26	COM19	COM30	COM29		–486		
283	COM39	COM27	COM19	COM31	COM30		–436		
284	COM40	COM28	COM20	COM32	COM31		–386		
285	COM41	COM29	COM20	COM33	COM32		–336		
286	COM42	COM30	COM21	COM34	COM33		–286		
287	COM43	COM31	COM21	COM35	COM34		–236		
288	COM44	COM32	COM22	COM36	COM35		–186		
289	COM45	COM33	COM22	COM37	COM36		–136		
290	COM46	COM34	COM23	COM38	COM37		–86		
291	COM47	COM35	COM23	COM39	COM38		–36		
292	COM48	COM36	COM24	COM40	COM39		14		
293	COM49	COM37	COM24	COM41	COM40		64		
294	COM50	COM38	COM25	COM42	COM41		114		
295	COM51	COM39	COM25	COM43	COM42		164		
296	COM52	COM40	COM26	COM44	COM43		214		
297	COM53	COM41	COM26	COM45	COM44		264		
298	COM54	COM42	COM27	COM46	COM45		314		
299	COM55	COM43	COM27	COM47	COM46		365		
300	COM56	COM44	COM28	COM48	COM47		415		
301	COM57	COM45	COM28	COM49	COM48		465		
302	COM58	COM46	COM29	COM50	COM49		515		
303	COM59	DUMMY32	COM29	COM51	COM50		565		
304	COM60	COM47	COM30	COM52	DUMMY29		615		
305	COM61	DUMMY33	COM30	COM53	COM51		665		
306	COM62	COMS	COM31	DUMMY28	DUMMY30		715		
307	COM63	DUMMY34	COM31	COMS	COMS		765		
308	COMS	DUMMY35	COMS	DUMMY29	DUMMY31		815		
309	DUMMY20	DUMMY36	DUMMY20	DUMMY30	DUMMY32		865		

6. PIN DESCRIPTIONS

Power Supply Pins

Pin Name	I/O	Function	No. of Pins
V_{DD}	Power Supply	Shared with the MPU power supply terminal V_{CC}.	13
V_{SS}	Power Supply	This is a 0V terminal connected to the system GND.	9
V_{SS2}	Power Supply	This is the reference power supply for the step-up voltage circuit for the liquid crystal drive.	4
V_{RS}	Power Supply	This is the externally-input V_{REG} power supply for the LCD power supply voltage regulator. These are only enabled for the models with the V_{REG} external input option.	2
V_1, V_2, V_3, V_4, V_5	Power Supply	This is a multi-level power supply for the liquid crystal drive. The voltage applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on V_{DD}, and must maintain the relative magnitudes shown below. V_{DD} (= V_0) ≥ V_1 ≥ V_2 ≥ V_3 ≥ V_4 ≥ V_5 Master operation: When the power supply turns ON, the internal power supply circuits produce the V_1 to V_4 voltages shown below. The voltage settings are selected using the LCD bias set command.	10

	S1D10605*****		S1D10606*****		S1D10607*****		S1D10608*****		S1D10609*****	
V_1	1/9•V_5	1/7•V_5	1/8•V_5	1/6•V_5	1/6•V_5	1/5•V_5	1/8•V_5	1/6•V_5	1/8•V_5	1/6•V_5
V_2	2/9•V_5	2/7•V_5	2/8•V_5	2/6•V_5	2/6•V_5	2/5•V_5	2/8•V_5	2/6•V_5	2/8•V_5	2/6•V_5
V_3	7/9•V_5	5/7•V_5	6/8•V_5	4/6•V_5	4/6•V_5	3/5•V_5	6/8•V_5	4/6•V_5	6/8•V_5	4/6•V_5
V_4	8/9•V_5	6/7•V_5	7/8•V_5	5/6•V_5	5/6•V_5	4/5•V_5	7/8•V_5	5/6•V_5	7/6•V_5	5/6•V_5

LCD Power Supply Circuit Terminals

Pin Name	I/O	Function	No. of Pins
CAP1+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1– terminal.	2
CAP1–	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.	2
CAP2+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2– terminal.	2
CAP2–	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2+ terminal.	2
CAP3–	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.	2
V_{OUT}	O	DC/DC voltage converter. Connect a capacitor between this terminal and V_{SS}.	2
V_R	I	Output voltage regulator terminal. Provides the voltage between V_{DD} and V_5 through a resistive voltage divider. These are only enabled when the V_5 voltage regulator internal resistors are not used (IRS = LOW). These cannot be used when the V_5 voltage regulator internal resistors are used (IRS = HIGH).	2

System Bus Connection Terminals

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>D7 to D0

(SI)
(SCL)</td><td>I/O</td><td>This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus.
When the serial interface is selected (P/S = LOW), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance.
When the chip select is inactive, D0 to D7 are set to high impedance.</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command.
A0 = HIGH: Indicates that D0 to D7 are display data.
A0 = LOW: Indicates that D0 to D7 are control data.</td><td>1</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>When $\overline{RES}$ is set to LOW, the settings are initialized.
The reset operation is performed by the $\overline{RES}$ signal level.</td><td>1</td></tr>
<tr><td>$\overline{CS1}$
CS2</td><td>I</td><td>This is the chip select signal. When $\overline{CS1}$ = LOW and CS2 = HIGH, then the chip select becomes active, and data/command I/O is enabled.</td><td>2</td></tr>
<tr><td>$\overline{RD}$
(E)</td><td>I</td><td>• When connected to an 8080 MPU, this is active LOW.
This pin is connected to the $\overline{RD}$ signal of the 8080 MPU, and the S1D10605 series data bus is in an output status when this signal is LOW.
• When connected to a 6800 Series MPU, this is active HIGH.
This is the 6800 Series MPU enable clock input terminal.</td><td>1</td></tr>
<tr><td>$\overline{WR}$
(R/$\overline{W}$)</td><td>I</td><td>• When connected to an 8080 MPU, this is active LOW.
This terminal connects to the 8080 MPU $\overline{WR}$ signal. The signals on the data bus are latched at the rising edge of the $\overline{WR}$ signal.
• When connected to a 6800 Series MPU:
This is the read/write control signal input terminal.
When R/$\overline{W}$ = HIGH: Read.
When R/$\overline{W}$ = LOW: Write.</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>This is the MPU interface switch terminal.
C86 = HIGH: 6800 Series MPU interface.
C86 = LOW: 8080 MPU interface.</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>This is the parallel data input/serial data input switch terminal.
P/S = HIGH: Parallel data input.
P/S = LOW: Serial data input.
The following applies depending on the P/S status:
<table><tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial Clock</th></tr><tr><td>HIGH</td><td>A0</td><td>D0 to D7</td><td>$\overline{RD}$, $\overline{WR}$</td><td></td></tr><tr><td>LOW</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr></table>
When P/S = LOW, D0 to D5 are HZ. D0 to D5 may be HIGH, LOW or Open.
$\overline{RD}$ (E) and $\overline{WR}$ (P/$\overline{W}$) are fixed to either HIGH or LOW.
With serial data input, RAM display data reading is not supported.</td><td>1</td></tr>
<tr><td>CLS</td><td>I</td><td>Terminal to select whether or enable or disable the display clock internal oscillator circuit.
CLS = HIGH: Internal oscillator circuit is enabled
CLS = LOW: Internal oscillator circuit is disabled (requires external input)
When CLS = LOW, input the display clock through the CL terminal.
When using the S1D10605 Series as a master or slave, set respective CLS pins at the same level.
<table><tr><th>Display clock</th><th>Master</th><th>Slave</th></tr><tr><td>Built-in oscillator circuit used</td><td>HIGH</td><td>HIGH</td></tr><tr><td>External input</td><td>LOW</td><td>LOW</td></tr></table></td><td>1</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>M/S</td><td>I</td><td>This terminal selects the master/slave operation for the S1D10605 Series chips. Master operation outputs the timing signals that are required for the LCD display, while slave operation inputs the timing signals required for the liquid crystal display, synchronizing the liquid crystal display system.
M/S = HIGH: Master operation
M/S = LOW: Slave operation
The following is true depending on the M/S and CLS status:
<table>
<tr><th>M/S</th><th>CLS</th><th>Oscillator Circuit</th><th>Power Supply Circuit</th><th>CL</th><th>FR</th><th>FRS</th><th>DOF</th></tr>
<tr><td>HIGH</td><td>HIGH
LOW</td><td>Enabled
Disabled</td><td>Enabled
Enabled</td><td>Output
Input</td><td>Output
Output</td><td>Output
Output</td><td>Output
Output</td></tr>
<tr><td>LOW</td><td>HIGH
LOW</td><td>Disabled
Disabled</td><td>Disabled
Disabled</td><td>Input
Input</td><td>Input
Input</td><td>Output
Output</td><td>Input
Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>CL</td><td>I/O</td><td>This is the display clock input terminal
The following is true depending on the M/S and CLS status.
<table>
<tr><th>M/S</th><th>CLS</th><th>CL</th></tr>
<tr><td>HIGH</td><td>HIGH
LOW</td><td>Output
Input</td></tr>
<tr><td>LOW</td><td>HIGH
LOW</td><td>Input
Input</td></tr>
</table>When the S1D10605 Series chips are used in master/slave mode, the various CL terminals must be connected.</td><td>1</td></tr>
<tr><td>FR</td><td>I/O</td><td>This is the liquid crystal alternating current signal I/O terminal.
M/S = HIGH: Output
M/S = LOW: Input
When the S1D10605 Series chip is used in master/slave mode, the various FR terminals must be connected.</td><td>1</td></tr>
<tr><td>$\overline{DOF}$</td><td>I/O</td><td>This is the liquid crystal display blanking control terminal.
M/S = HIGH: Output
M/S = LOW: Input
When the S1D10605 Series chip is used in master/slave mode, the various $\overline{DOF}$ terminals must be connected.</td><td>1</td></tr>
<tr><td>FRS</td><td>O</td><td>This is the output terminal for the static drive.
This terminal is only enabled when the static indicator display is ON when in master operation mode, and is used in conjunction with the FR terminal.</td><td>1</td></tr>
<tr><td>IRS</td><td>I</td><td>This terminal selects the resistors for the V_5 voltage level adjustment.
IRS = HIGH: Use the internal resistors
IRS = LOW: Do not use the internal resistors. The V_5 voltage level is regulated by an external resistive voltage divider attached to the V_R terminal.
This pin is enabled only when the master operation mode is selected.
It is fixed to either HIGH or LOW when the slave operation mode is selected.</td><td>1</td></tr>
<tr><td>$\overline{HPM}$</td><td>I</td><td>This is the power control terminal for the power supply circuit for liquid crystal drive.
$\overline{HPM}$ = HIGH: Normal mode
$\overline{HPM}$ = LOW: High power mode
This pin is enabled only when the master operation mode is selected.
It is fixed to either HIGH or LOW when the slave operation mode is selected.</td><td>1</td></tr>
</table>

Liquid Crystal Drive Terminals

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>SEG0
to
SEG131</td><td>O</td><td>These are the liquid crystal segment drive outputs. Through a combination of the contents of the display RAM and with the FR signal, a single level is selected from VDD, V2, V3, and V5.
<table>
<tr><th>RAM DATA</th><th>FR</th><th colspan="2">Output Voltage</th></tr>
<tr><td></td><td></td><td>Normal Display</td><td>Reverse Display</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>VDD</td><td>V2</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>V5</td><td>V3</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>V2</td><td>VDD</td></tr>
<tr><td>LOW</td><td>LOW</td><td>V3</td><td>V5</td></tr>
<tr><td>Power save</td><td>—</td><td colspan="2">VDD</td></tr>
</table></td><td>132</td></tr>
<tr><td>COM0
to
COMn</td><td>O</td><td>These are the liquid crystal common drive outputs.
<table>
<tr><th>Part No.</th><th>COM</th></tr>
<tr><td>S1D10605*****</td><td>COM 0 ~ COM 63</td></tr>
<tr><td>S1D10606*****</td><td>COM 0 ~ COM 47</td></tr>
<tr><td>S1D10607*****</td><td>COM 0 ~ COM 31</td></tr>
<tr><td>S1D10608*****</td><td>COM 0 ~ COM 53</td></tr>
<tr><td>S1D10609*****</td><td>COM 0 ~ COM 51</td></tr>
</table>
<table>
<tr><th>Part No.</th><th></th></tr>
<tr><td>S1D10605*****</td><td>64</td></tr>
<tr><td>S1D10606*****</td><td>48</td></tr>
<tr><td>S1D10607*****</td><td>32</td></tr>
<tr><td>S1D10608*****</td><td>54</td></tr>
<tr><td>S1D10609*****</td><td>52</td></tr>
</table>
Through a combination of the contents of the scan data and with the FR signal, a single level is selected from VDD, V1, V4, and V5.
<table>
<tr><th>Scan Data</th><th>FR</th><th>Output Voltage</th></tr>
<tr><td>HIGH</td><td>HIGH</td><td>V5</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>VDD</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>V1</td></tr>
<tr><td>LOW</td><td>LOW</td><td>V4</td></tr>
<tr><td>Power Save</td><td>—</td><td>VDD</td></tr>
</table></td><td></td></tr>
<tr><td>COMS</td><td>O</td><td>These are the COM output terminals for the indicator. Both terminals output the same signal.
Leave these open if they are not used.
When in master/slave mode, the same signal is output by both master and slave.</td><td>2</td></tr>
</table>

Test Terminals

Pin Name	I/O	Function	No. of Pins
TEST0 to 4 TEST7 to A	I/O	These are terminals for IC chip testing. They are set to OPEN.	12
TEST5, 6	I	These are terminals for IC chip testing. They are set to VDD or OPEN.	2

Total: 289 pins for the S1D10605*****.
273 pins for the S1D10606*****.
257 pins for the S1D10607*****.
279 pins for the S1D10608*****.
277 pins for the S1D10609*****.

7. FUNCTION DESCRIPTION

The MPU Interface

Selecting the Interface Type

With the S1D10605 Series chips, data transfers are done through an 8-bit bi-directional data bus (D7 to D0) or through a serial data input (SI). Through selecting the P/S terminal polarity to the HIGH or LOW it is possible to select either parallel data input or serial data input as shown in Table 1.

Table 1

P/S	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5~D0
HIGH: Parallel Input	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5~D0
LOW: Serial Input	CS1	CS2	A0	—	—	—	SI	SCL	(HZ)

"—" indicates fixed to either HIGH or to LOW

The Parallel Interface

When the parallel interface has been selected (P/S = HIGH), then it is possible to connect directly to either an 8080-system MPU or a 6800 Series MPU (as shown in Table 2) by selecting the C86 terminal to either HIGH or to LOW.

Table 2

P/S	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7~D0
HIGH: 6800 Series MPU Bus	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	D7~D0
LOW: 8080 MPU Bus	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7~D0

Moreover, data bus signals are recognized by a combination of A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$) signals, as shown in Table 3.

Table 3

Shared	6800 Series	8080 Series		Function
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads the display data
1	0	1	0	Writes the display data
0	1	0	1	Status read
0	0	1	0	Write control data (command)

The Serial Interface

When the serial interface has been selected (P/S = LOW) then when the chip is in active state ($\overline{CS1}$ = LOW and CS2 = HIGH) the serial data input (SI) and the serial clock input (SCL) can be received. The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of the eighth serial clock for the processing.
The A0 input is used to determine whether or the serial data input is display data or command data; when A0 = HIGH, the data is display data, and when A0 = LOW then the data is command data. The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active.
Figure 1 is a serial interface signal chart.

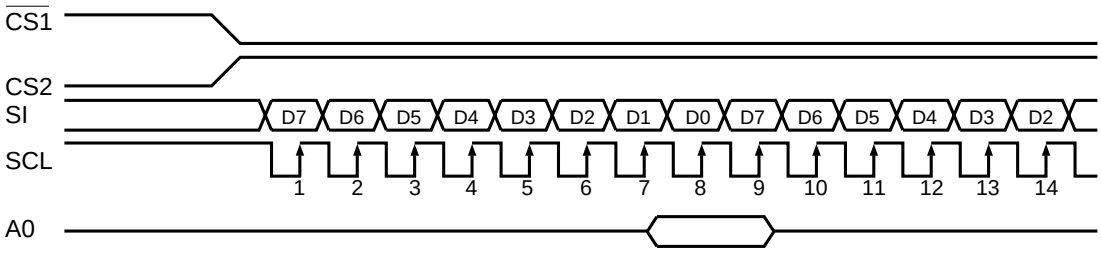


Figure 1

* When the chip is not active, the shift registers and the counter are reset to their initial states.
* Reading is not possible while in serial interface mode.
* Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend that operation be rechecked on the actual equipment.

The Chip Select

The S1D10605 Series chips have two chip select terminals: $\overline{CS1}$ and CS2. The MPU interface or the serial interface is enabled only when $\overline{CS1}$ = LOW and CS2 = HIGH.
When the chip select is inactive, D0 to D7 enter a high impedance state, and the A0, $\overline{RD}$, and $\overline{WR}$ inputs are inactive. When the serial interface is selected, the shift register and the counter are reset.

Accessing the Display Data RAM and the Internal Registers

Data transfer at a higher speed is ensured since the MPU is required to satisfy the cycle time (t_{CYC}) requirement alone in accessing the S1D10605 Series. Wait time may not be considered.
And, in the S1D10605 Series chips, each time data is sent from the MPU, a type of pipeline process between LSIs is performed through the bus holder attached to the internal data bus.
For example, when the MPU writes data to the display data RAM, once the data is stored in the bus holder, then it is written to the display data RAM before the next data write cycle. Moreover, when the MPU reads the display data RAM, the first data read cycle (dummy) stores the read data in the bus holder, and then the data is read from the bus holder to the system bus at the next data read cycle.
There is a certain restriction in the read sequence of the display data RAM. Please be advised that data of the specified address is not generated by the read instruction issued immediately after the address setup. This data is generated in data read of the second time. Thus, a dummy read is required whenever the address setup or write cycle operation is conducted.
This relationship is shown in Figure 2.

The Busy Flag

When the busy flag is "1" it indicates that the S1D10605 Series chip is running internal processes, and at this time no command aside from a status read will be received. The busy flag is outputted to D7 pin with the read instruction. If the cycle time (t_{CYC}) is maintained, it is not necessary to check for this flag before each command. This makes vast improvements in MPU processing capabilities possible.

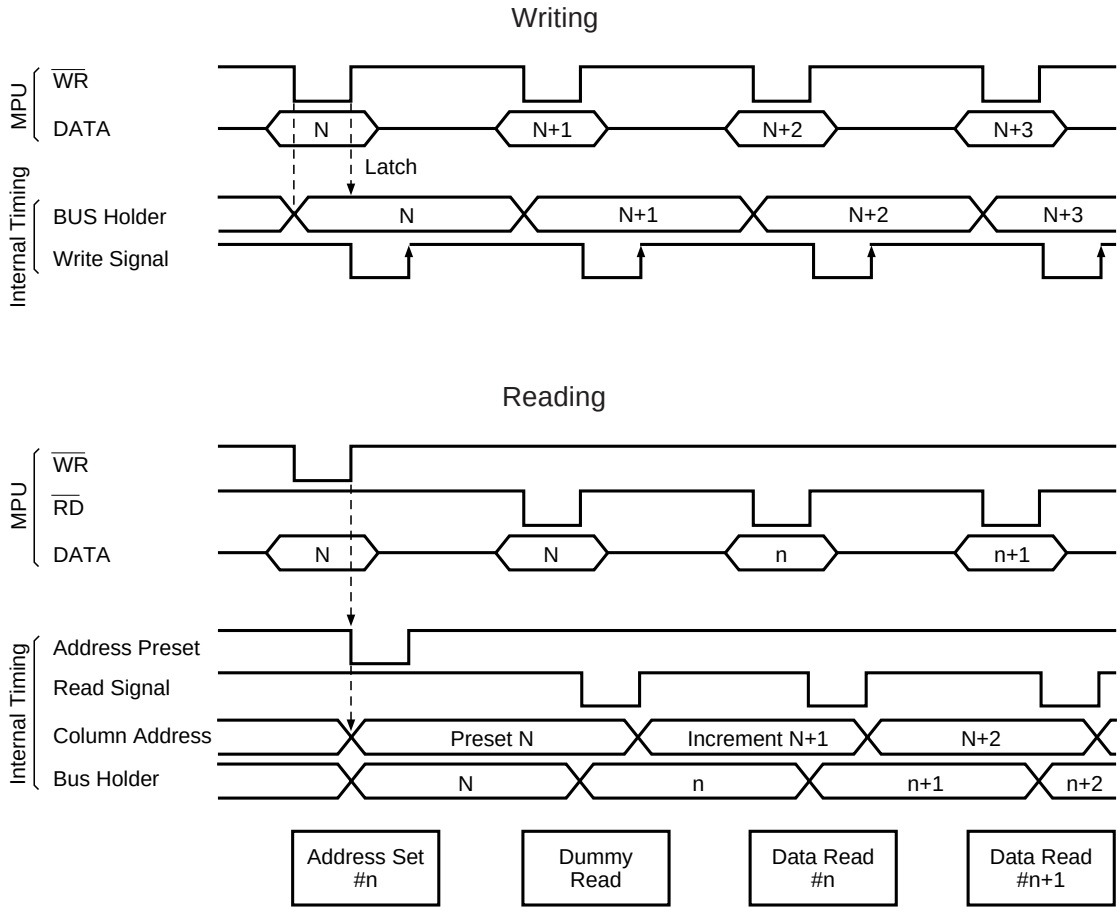


Figure 2

Display Data RAM

Display Data RAM

The display data RAM is a RAM that stores the dot data for the display. It has a 65 (8 page × 8 bit +1) × 132 bit structure. It is possible to access the desired bit by specifying the page address and the column address.
Because, as is shown in Figure 3, the D7 to D0 display data from the MPU corresponds to the liquid crystal display common direction, there are few constraints at the time of display data transfer when multiple S1D10605 series chips are used, thus and display structures can be created easily and with a high degree of freedom.
Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, it will not cause adverse effects on the display (such as flickering).

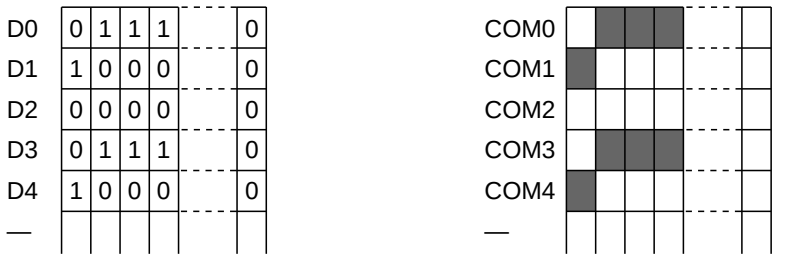


Figure 3

The Page Address Circuit

As shown in Figure 6-4, page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access.
Page address 8 (D3, D2, D1, D0 = 1, 0, 0, 0) is the page for the RAM region used only by the indicators, and only display data D0 is used.

The Column Addresses

As is shown in Figure 4, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously.
Moreover, the incrementation of column addresses stops with 83H. Because the column address is independent of the page address, when moving, for example, from page 0 column 83H to page 1 column 00H, it is necessary to respecify both the page address and the column address.
Furthermore, as is shown in Table 4, the ADC command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the LCD module is assembled can be minimized.

Table 4

SEG Output	SEG0		SEG 131
ADC "0"	0 (H) →	Column Address	→ 83 (H)
(D0) "1"	83 (H) ←	Column Address	← 0 (H)

The Line Address Circuit

The line address circuit, as shown in Table 4, specifies the line address relating to the COM output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified (this is the COM0 output when the common output mode is normal, and the COM63 output for S1D10605 Series, COM47 output for S1D10606 Series, COM31 output for the S1D10607, COM53 output for the S1D10608 and COM51 output for the S1D10609 Series when the common output mode is reversed. The display area is a 65 line area for the S1D10605 Series, a 49 line area for the S1D10606, a 33 line area for the S1D10607, a 55 line area for the S1D10608 and a 53 line area for the S1D10609 from the display start line address.
If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. can be performed.

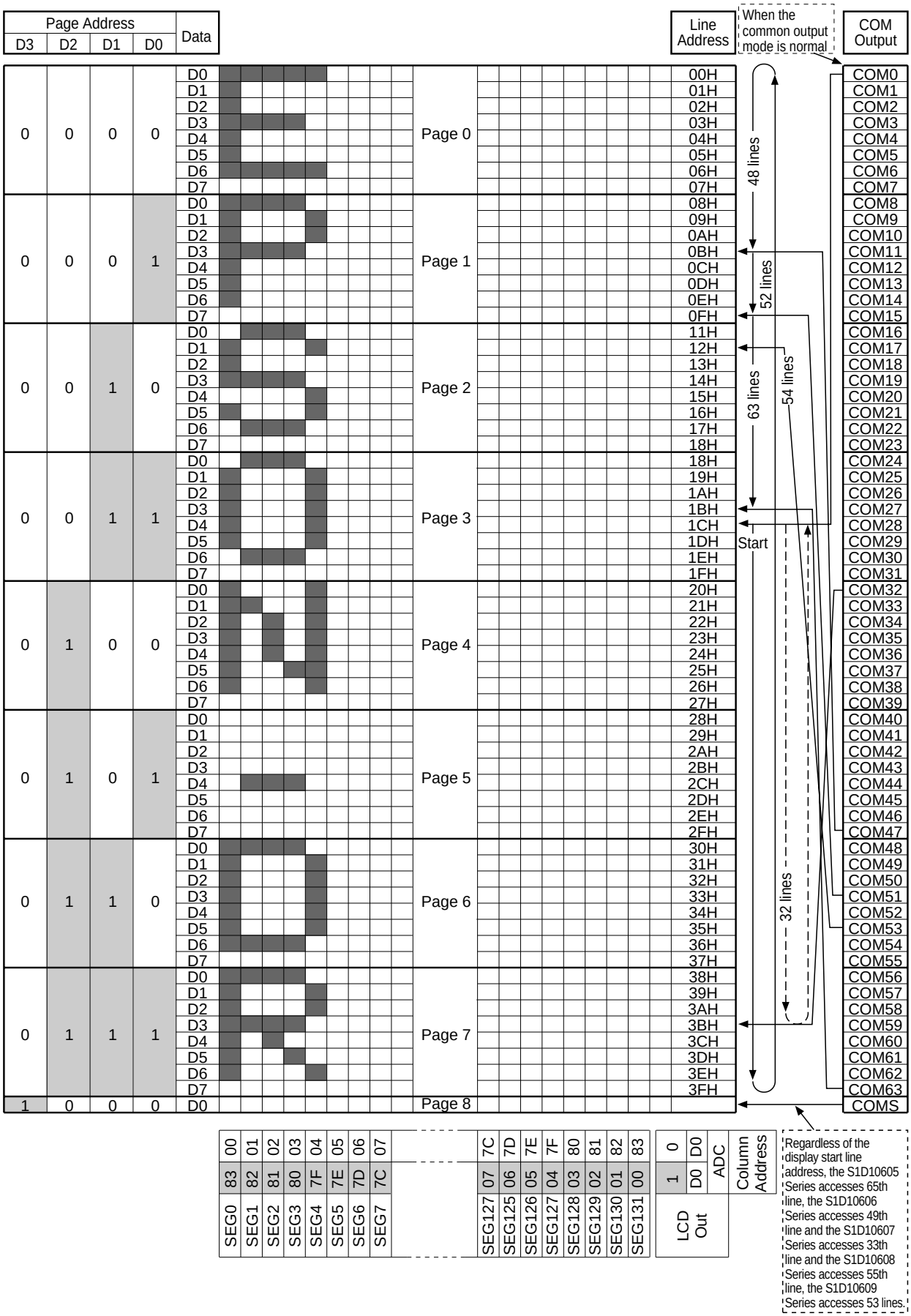

Page Address
D3 D2 D1 D0
Data
Line Address
When the common output mode is normal
COM Output
Page 0
Page 1
Page 2
Page 3
Page 4
Page 5
Page 6
Page 7
Page 8
48 lines
52 lines
54 lines
63 lines
32 lines
Start
COM0 COM1 COM2 COM3 COM4 COM5 COM6 COM7 COM8 COM9 COM10 COM11 COM12 COM13 COM14 COM15 COM16 COM17 COM18 COM19 COM20 COM21 COM22 COM23 COM24 COM25 COM26 COM27 COM28 COM29 COM30 COM31 COM32 COM33 COM34 COM35 COM36 COM37 COM38 COM39 COM40 COM41 COM42 COM43 COM44 COM45 COM46 COM47 COM48 COM49 COM50 COM51 COM52 COM53 COM54 COM55 COM56 COM57 COM58 COM59 COM60 COM61 COM62 COM63 COMS
SEG0 SEG1 SEG2 SEG3 SEG4 SEG5 SEG6 SEG7
SEG127 SEG125 SEG126 SEG127 SEG128 SEG129 SEG130 SEG131
LCD Out
ADC
Column Address
Regardless of the display start line address, the S1D10605 Series accesses 65th line, the S1D10606 Series accesses 49th line and the S1D10607 Series accesses 33th line and the S1D10608 Series accesses 55th line, the S1D10609 Series accesses 53 lines.

Figure 4

The Display Data Latch Circuit

The display data latch circuit is a latch that temporarily stores the display data that is output to the liquid crystal driver circuit from the display data RAM.
Because the display normal/reverse status, display ON/OFF status, and display all points ON/OFF commands control only the data within the latch, they do not change the data within the display data RAM itself.

The Oscillator Circuit

This is a CR-type oscillator that produces the display clock. The oscillator circuit is only enabled when M/S = HIGH and CLS = HIGH.
When CLS = LOW the oscillation stops, and the display clock is input through the CL terminal.

Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading to the display data liquid crystal driver circuits is completely independent of accesses to the display data RAM by the MPU. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, there is absolutely no adverse effect (such as flickering) on the display.
Moreover, the display timing generator circuit generates the common timing and the liquid crystal alternating current signal (FR) from the display clock. It generates a drive wave form using a 2 frame alternating current drive method, as is shown in Figure 5, for the liquid crystal drive circuit.

Two-frame alternating current drive wave form (S1D10605*****)

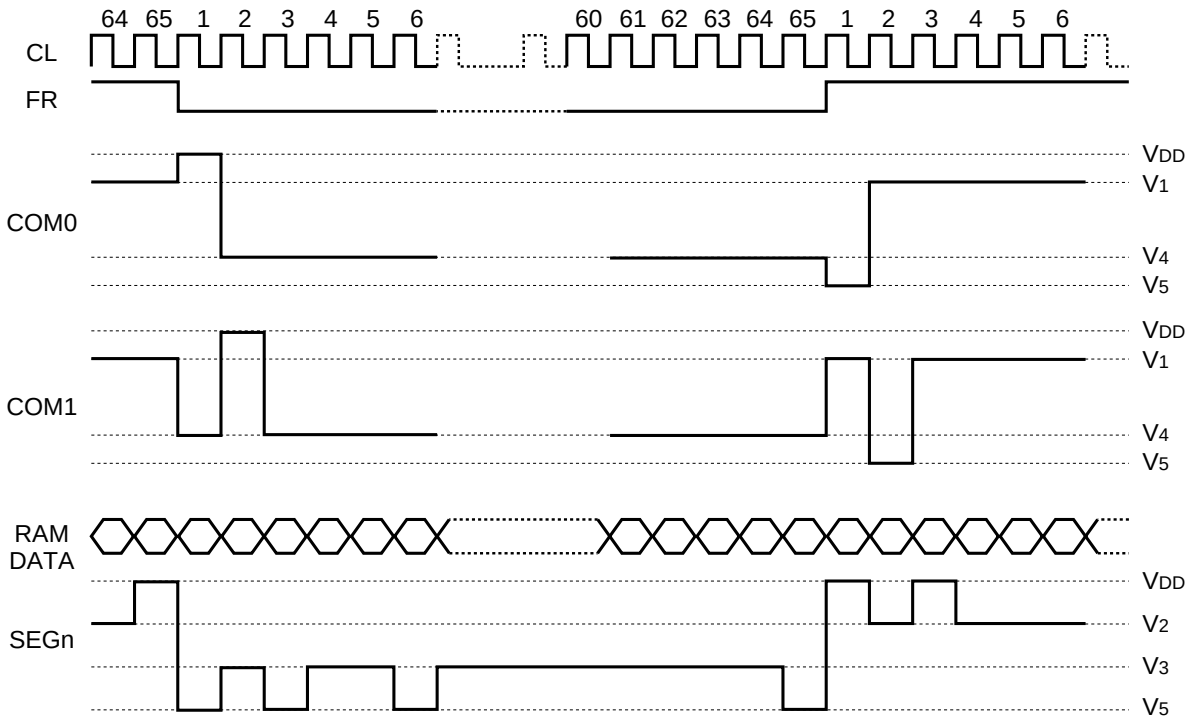


Figure 5

When multiple S1D10605 Series chips are used, the slave chips must be supplied the display timing signals (FR, CL, $\overline{DOF}$) from the master chip[s].
Table 5 shows the status of the FR, CL, and $\overline{DOF}$ signals.

Table 5

Operating Mode		FR	CL	$\overline{DOF}$
Master (M/S = HIGH)	The internal oscillator circuit is enabled (CLS = HIGH)	Output	Output	Output
	The internal oscillator circuit is disabled (CLS = LOW)	Output	Input	Output
Slave (M/S = LOW)	Set the CLS pin to the same level as with the master.	Input	Input	Input
		Input	Input	Input

The Common Output Status Select Circuit

In the S1D10605 Series chips, the COM output scan direction can be selected by the common output status select command. (See Table 6.) Consequently, the constraints in IC layout at the time of LCD module assembly can be minimized.

Table 6

Status	COM Scan Direction				
	S1D10605***	**S1D10606*****	**S1D10607*****	**S1D10608*****	**S1D10609*****
Normal	COM0 → COM63	COM0 → COM47	COM0 → COM31	COM0 → COM53	COM0 → COM51
Reverse	COM63 → COM0	COM47 → COM0	COM31 → COM0	COM53 → COM0	COM51 → COM0

The Liquid Crystal Driver Circuits

These are a 197-channel (S1D10605 Series), a 181-channel (S1D10606 Series) multiplexers 165-channel (S1D10607 Series), a 187-channel (S1D10608 Series). and a 185-channel (S1D10609 Series) that generate four voltage levels for driving the liquid crystal. The combination of the display data, the COM scan signal, and the FR signal produces the liquid crystal drive voltage output.
Figure 6 shows examples of the SEG and COM output wave form.

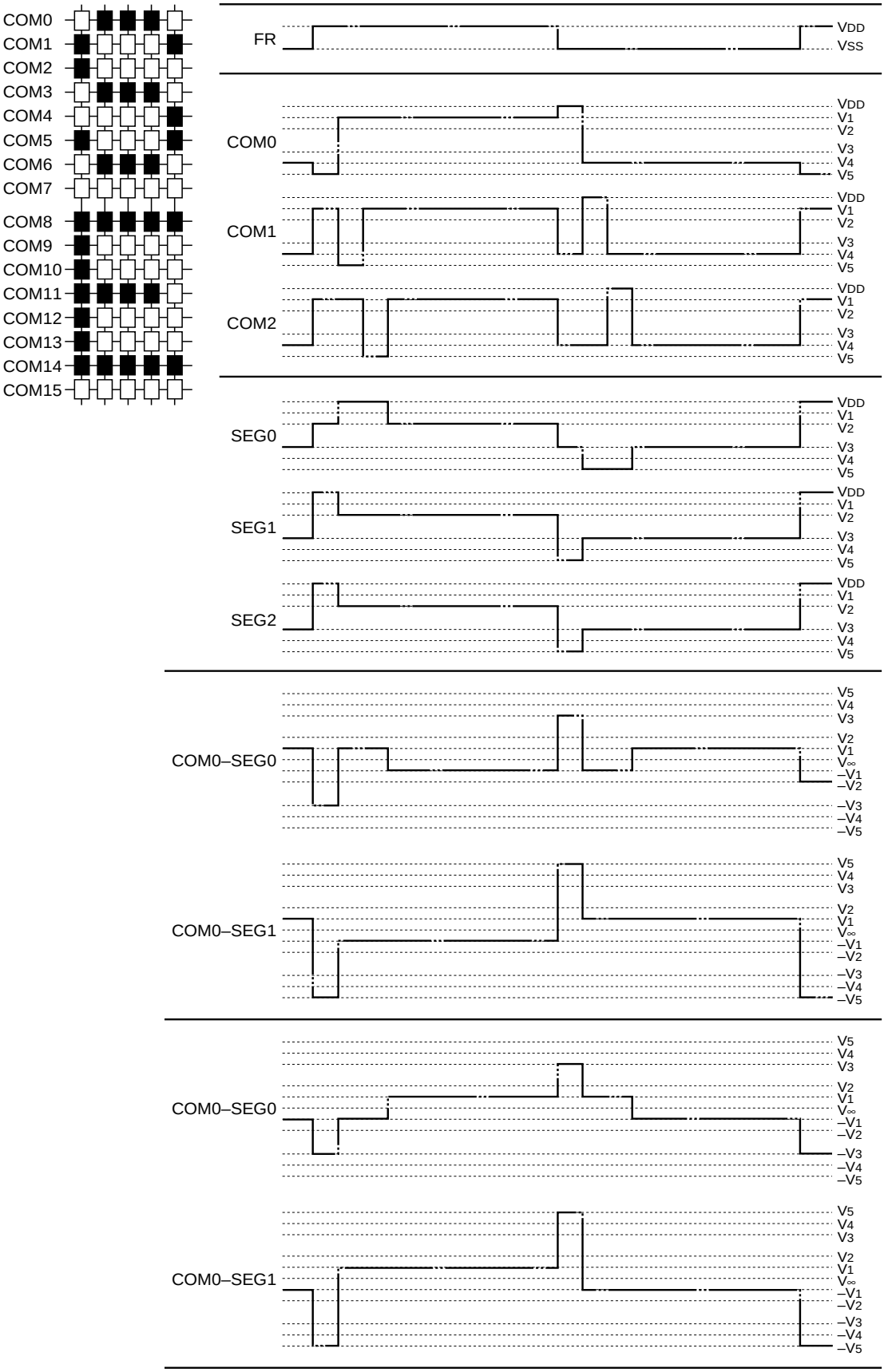

COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10
COM11
COM12
COM13
COM14
COM15
FR
VDD
VSS
COM0
COM1
COM2
V1
V2
V3
V4
V5
SEG0
SEG1
SEG2
COM0–SEG0
COM0–SEG1
V∞
–V1
–V2
–V3
–V4
–V5

Figure 6

The Power Supply Circuits

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for the liquid crystal drivers. They comprise Booster circuits, voltage regulator circuits, and voltage follower circuits. They are only enabled in master operation.

The power supply circuits can turn the Booster circuits, the voltage regulator circuits, and the voltage follower circuits ON of OFF independently through the use of the Power Control Set command. Consequently, it is possible to make an external power supply and the internal power supply function somewhat in parallel. Table 7 shows the Power Control Set Command 3-bit data control function, and Table 8 shows reference combinations.

Table 7 The Control Details of Each Bit of the Power Control Set Command

Item	Status "1"	Status "0"
D2 Booster circuit control bit	ON	OFF
D1 Voltage regulator circuit (V regulator circuit) control bit	ON	OFF
D0 Voltage follower circuit (V/F circuit) control bit	ON	OFF

Table 8 Reference Combinations

Use Settings	D2	D1	D0	Step-up circuit	V regulator circuit	V/F circuit	External voltage input	Step-up voltage system terminal
① Only the internal power supply is used	1	1	1	O	O	O	V_{SS2}	Used
② Only the V regulator circuit and the V/F circuit are used	0	1	1	X	O	O	V_{OUT}, V_{SS2}	Open
③ Only the V/F circuit is used	0	0	1	X	X	O	V_5, V_{SS2}	Open
④ Only the external power supply is used	0	0	0	X	X	X	V_1 to V_5	Open

* The "step-up system terminals" refer CAP1+, CAP1–, CAP2+, CAP2–, and CAP3–.

* While other combinations, not shown above, are also possible, these combinations are not recommended because they have no practical use.

The Step-up Voltage Circuits

Using the step-up voltage circuits equipped within the S1D10605 Series chips it is possible to product a Quad step-up, a Triple step-up, and a Double step-up of the V_{DD} – V_{SS2} voltage levels.

Quad step-up: Connect capacitor C_1 between CAP1+ and CAP1–, between CAP2+ and CAP2–, between CAP1+ and CAP3–, and between V_{SS2} and V_{OUT}, to produce a voltage level in the negative direction at the V_{OUT} terminal that is 4 times the voltage level between V_{DD} and V_{SS2}.

Triple step-up: Connect capacitor C_1 between CAP1+ and CAP1–, between CAP2+ and CAP2– and between V_{SS2} and V_{OUT}, and short between CAP3– and V_{OUT} to produce a voltage level in the negative direction at the V_{OUT} terminal that is 3 times the voltage difference between V_{DD} and V_{SS2}.

Double step-up: Connect capacitor C_1 between CAP1+ and CAP1–, and between V_{SS2} and V_{OUT}, leave CAP2+ open, and short between CAP2–, CAP3– and V_{OUT} to produce a voltage in the negative direction at the V_{OUT} terminal that is twice the voltage between V_{DD} and V_{SS2}.

The step-up voltage relationships are shown in Figure 7.

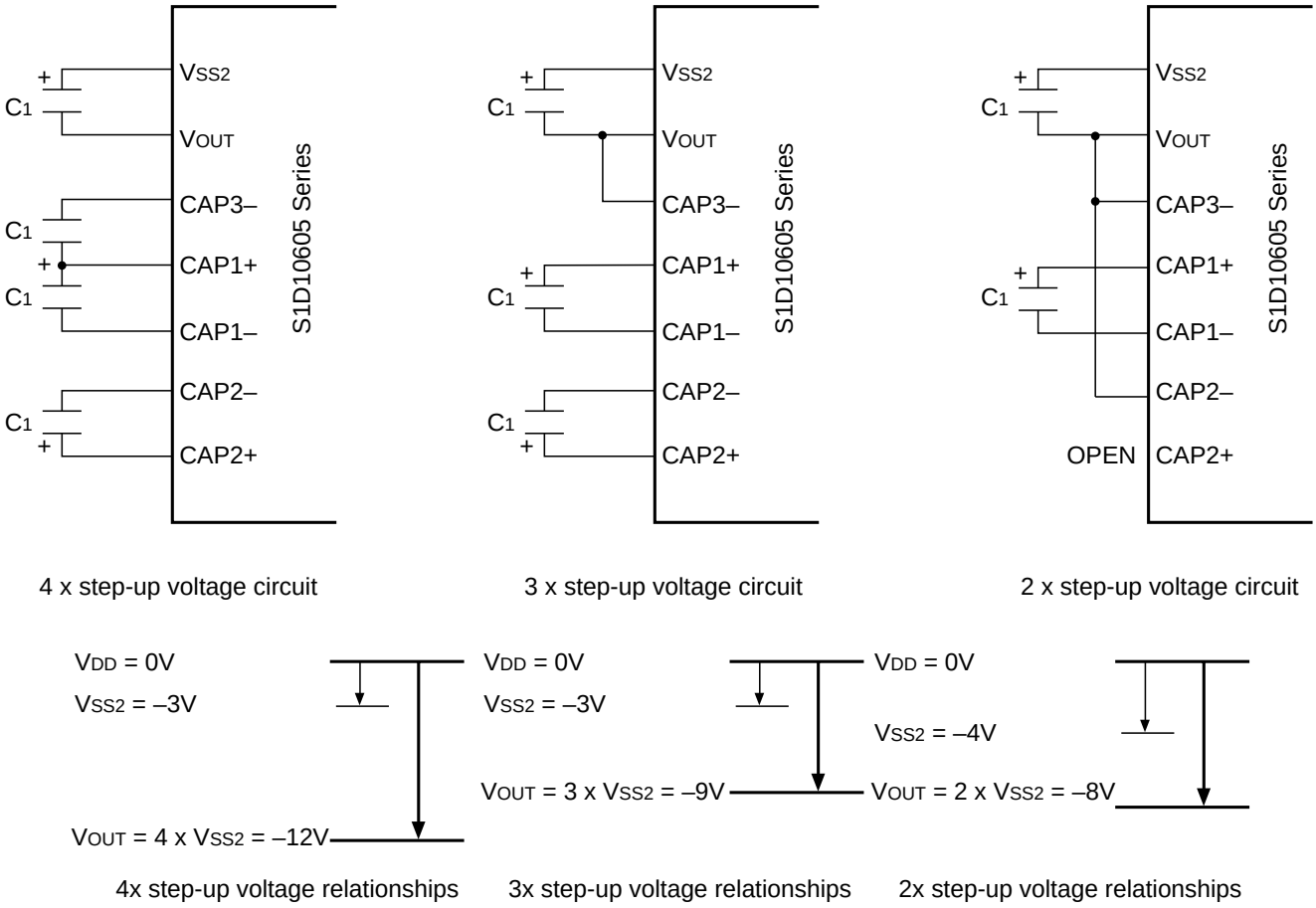


Figure 7

* The V_{SS2} voltage range must be set so that the V_{OUT} terminal voltage does not exceed the absolute maximum rated value.
* Low V_{DD} - V_{SS} voltage causes decrease in efficiency of step-up. Usage above 2.4V for V_{DD} - V_{SS} is recommended.

The Voltage Regulator Circuit

The step-up voltage generated at V_{OUT} outputs the liquid crystal driver voltage V_5 through the voltage regulator circuit.
Because the S1D10605 Series chips have an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V_5 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components.
Moreover, in the S1D10605 Series, thermal gradients have been prepared as V_{REG} options: approximately -0.05%/°C.

(A) When the V_5 Voltage Regulator Internal Resistors Are Used

Through the use of the V_5 voltage regulator internal resistors and the electronic volume function the liquid crystal power supply voltage V_5 can be controlled by commands alone (without adding any external resistors), making it possible to adjust the liquid crystal display brightness. The V_5 voltage can be calculated using equation A-1 over the range where $|V_5| < |V_{OUT}|$.

$$V_5 = \left(1 + \frac{Rb}{Ra}\right) \cdot V_{EV}$$
$$= \left(1 + \frac{Rb}{Ra}\right) \cdot \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG}$$
$$\left[\because V_{EV} = \left(1 - \alpha/162\right) \cdot V_{REG}\right] \qquad \text{(Equation A-1)}$$

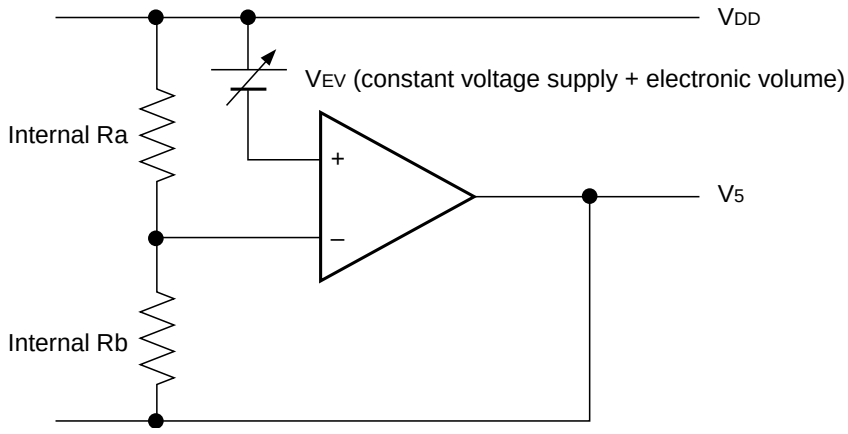


Figure 8

VREG is the IC-internal fixed voltage supply, and its voltage at Ta = 25°C is as shown in Table 9.

Table 9

Equipment Type	Thermal Gradient	Units	VREG	Units
Internal Power Supply	–0.05	[%/°C]	–2.1	[V]

α is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume register. Table 10 shows the value for α depending on the electronic volume register settings.

Table 10

D5	D4	D3	D2	D1	D0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
			⋮			⋮
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

Rb/Ra is the V5 voltage regulator internal resistor ratio, and can be set to 8 different levels through the V5 voltage regulator internal resistor ratio set command. The (1 + Rb/Ra) ratio assumes the values shown in Table 11 depending on the 3-bit data settings in the V5 voltage regulator internal resistor ratio register.

V_5 voltage regulator internal resistance ratio register value and (1 + Rb/Ra) ratio (Reference value)

Table 11

Register			S1D10605*****	S1D10606*****
			Equipment Type by Thermal Gradient [Units: %/°C]	Equipment Type by Thermal Gradient [Units: %/°C]
D2	D1	D0	–0.05	–0.05
0	0	0	3.0	3.0
0	0	1	3.5	3.5
0	1	0	4.0	4.0
0	1	1	4.5	4.5
1	0	0	5.0	5.0
1	0	1	5.5	5.4
1	1	0	6.0	5.9
1	1	1	6.4	6.4

Register			S1D10607*****	S1D10608*****/S1D10609*****
			Equipment Type by Thermal Gradient [Units: %/°C]	Equipment Type by Thermal Gradient [Units: %/°C]
D2	D1	D0	–0.05	–0.05
0	0	0	3.0	3.0
0	0	1	3.5	3.5
0	1	0	4.0	4.0
0	1	1	4.5	4.5
1	0	0	5.0	5.0
1	0	1	5.4	5.4
1	1	0	5.9	5.9
1	1	1	6.4	6.4

For the internal resistance ratio, a manufacturing dispersion of up to ±7% should be taken into account. When not within the tolerance, adjust the V_5 voltage by externally mounting Ra and Rb.
Figs. 9 (for S1D10605 Series), Figs. 10 (for S1D10606 Series) Figs. 11 (for S1D10607 Series), Figs.12 (for S1D 10608*****) and Figs. 13 (for S1D10609 Series). show V_5 voltage measured by values of the internal resistance ratio resistor for V_5 voltage adjustment and electric volume resister for each temperature grade model, when Ta = 25 °C.

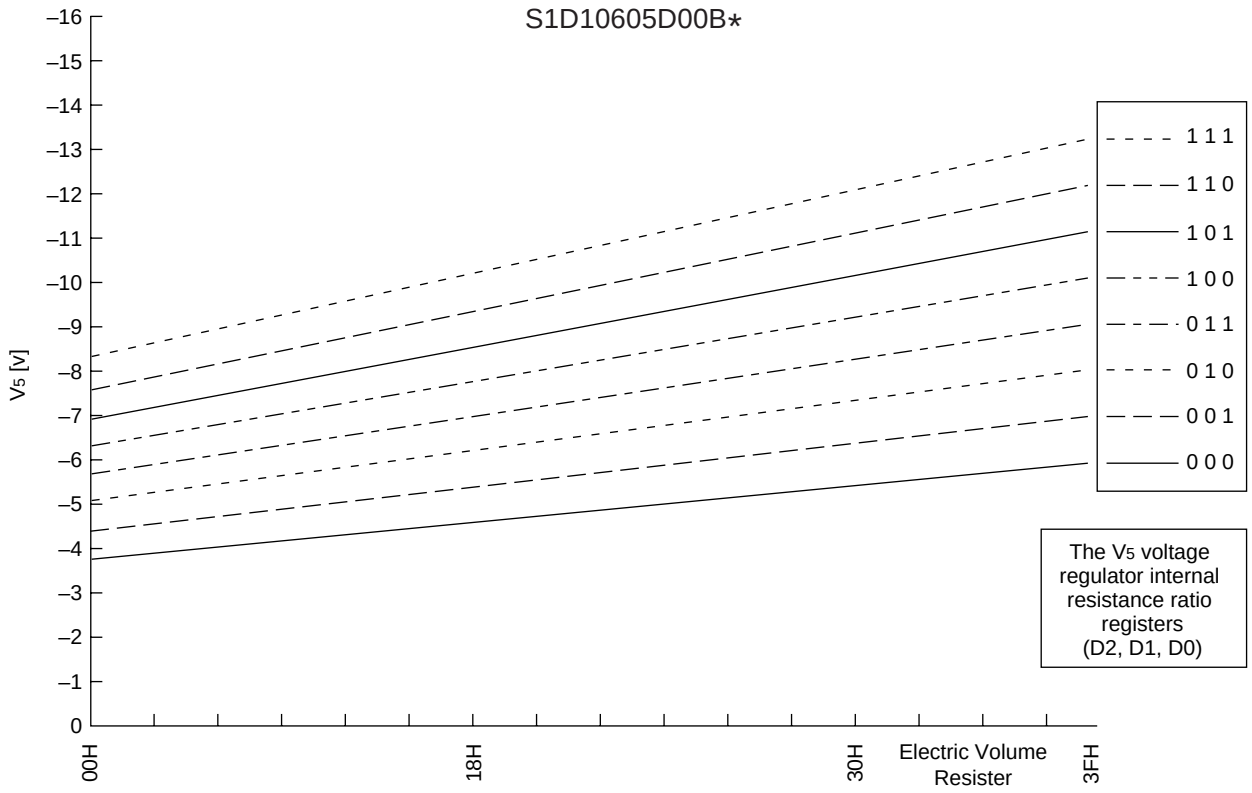


Figure 9: S1D10605D00B* For Models Where the Thermal Gradient = –0.05%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

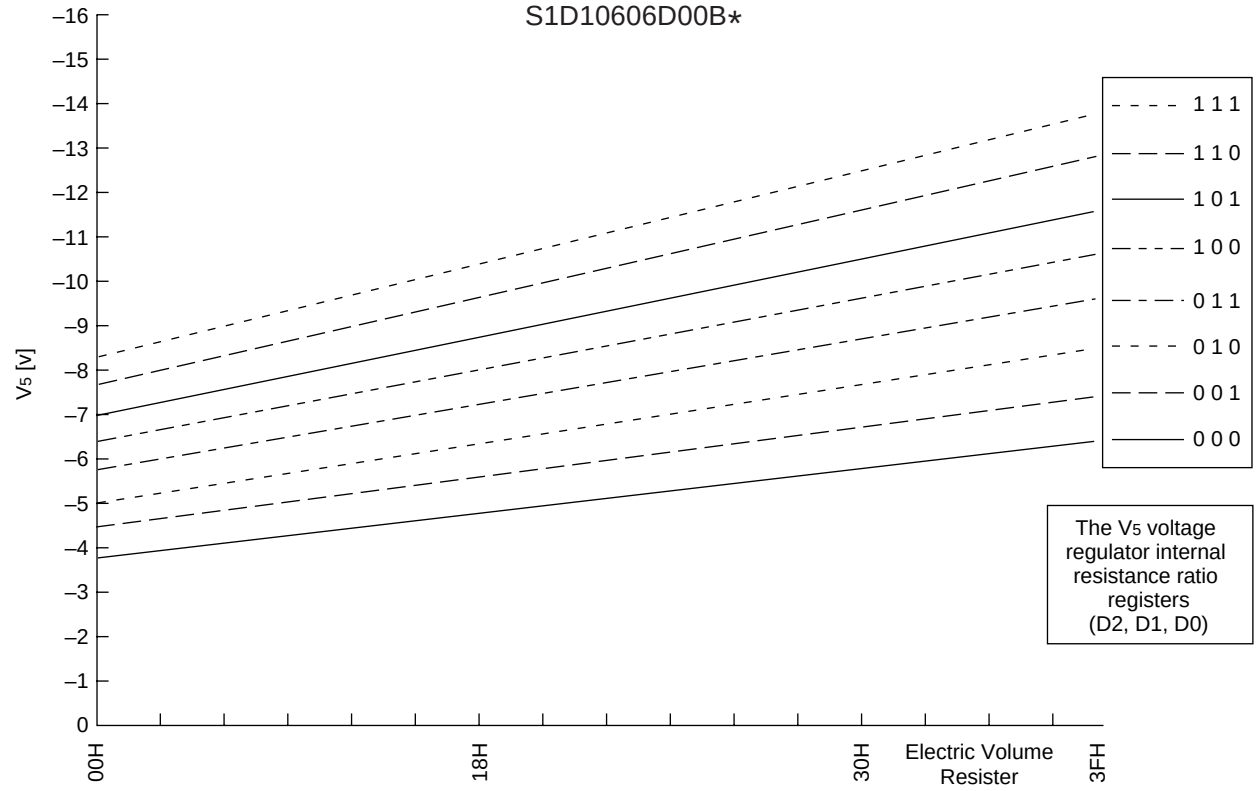


Figure 10: S1D10606D00B* For Models Where the Thermal Gradient = –0.05%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

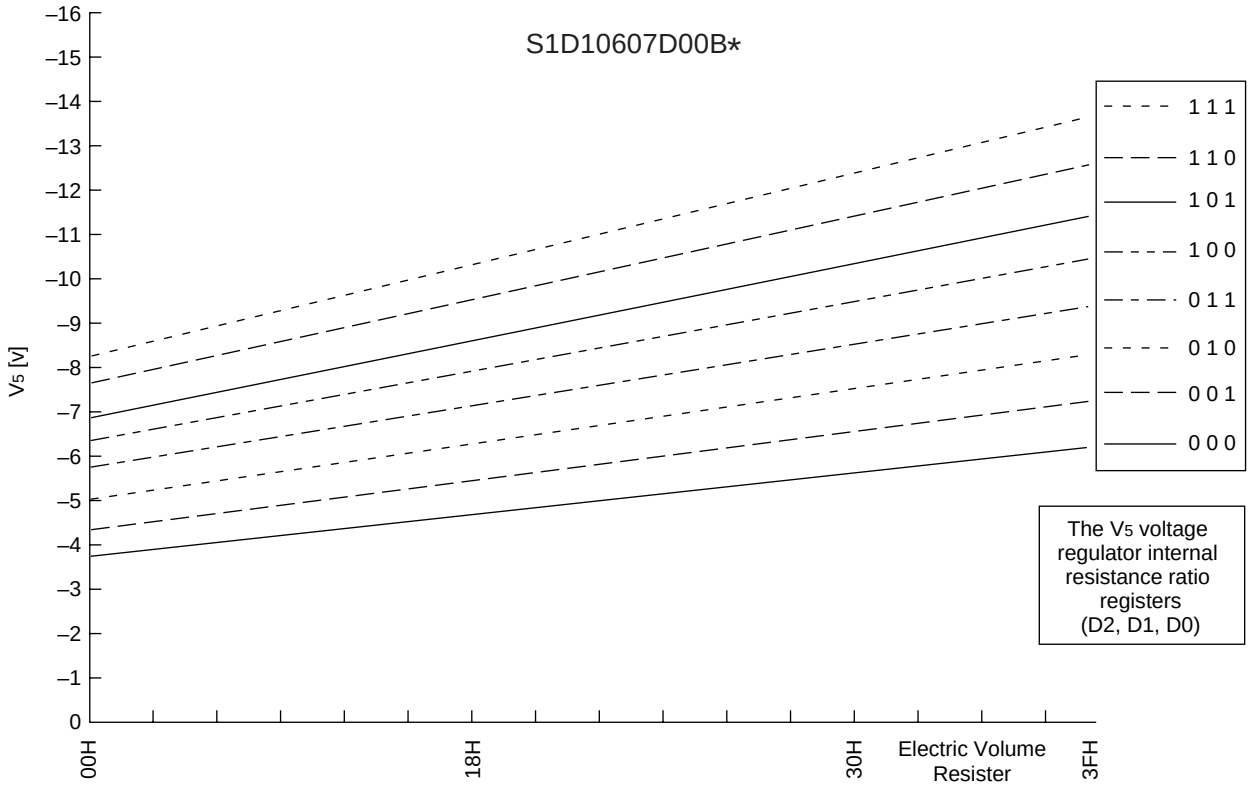


Figure 11: S1D10607D00B* For Models Where the Thermal Gradient = –0.05%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

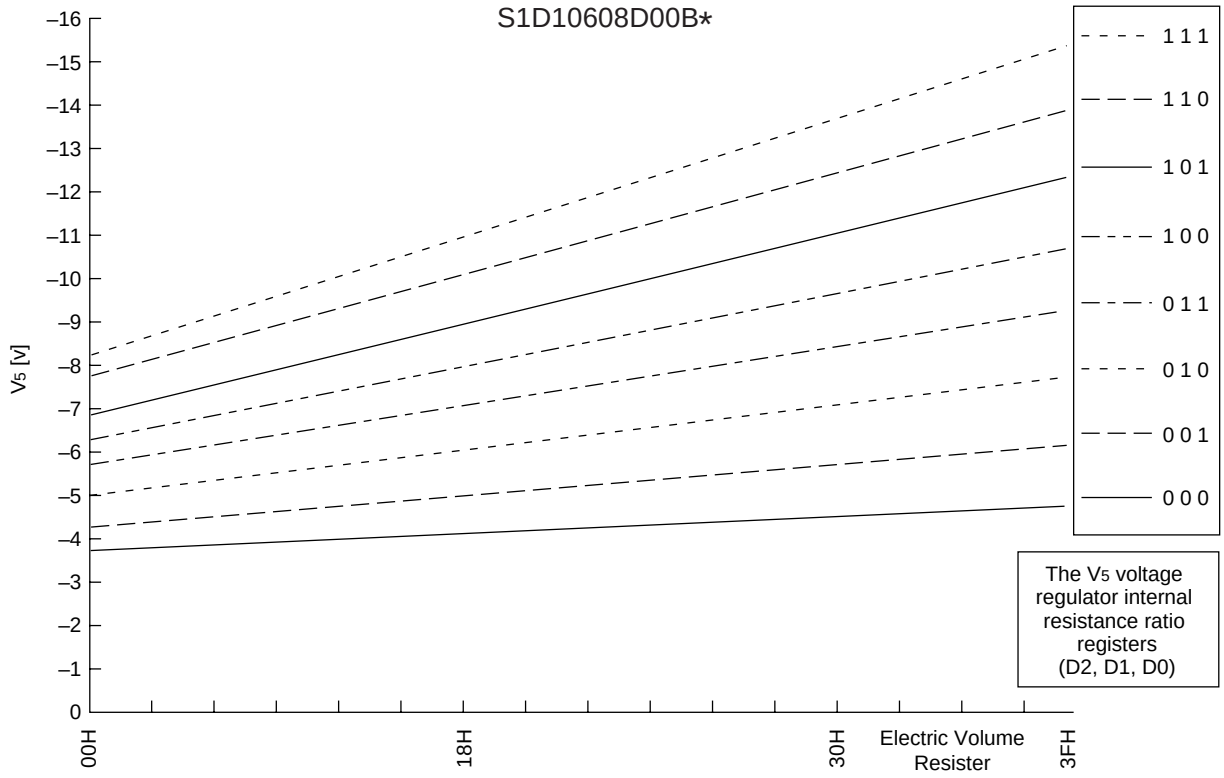


Figure 12: S1D10608D00B* For Models Where the Thermal Gradient = –0.05%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

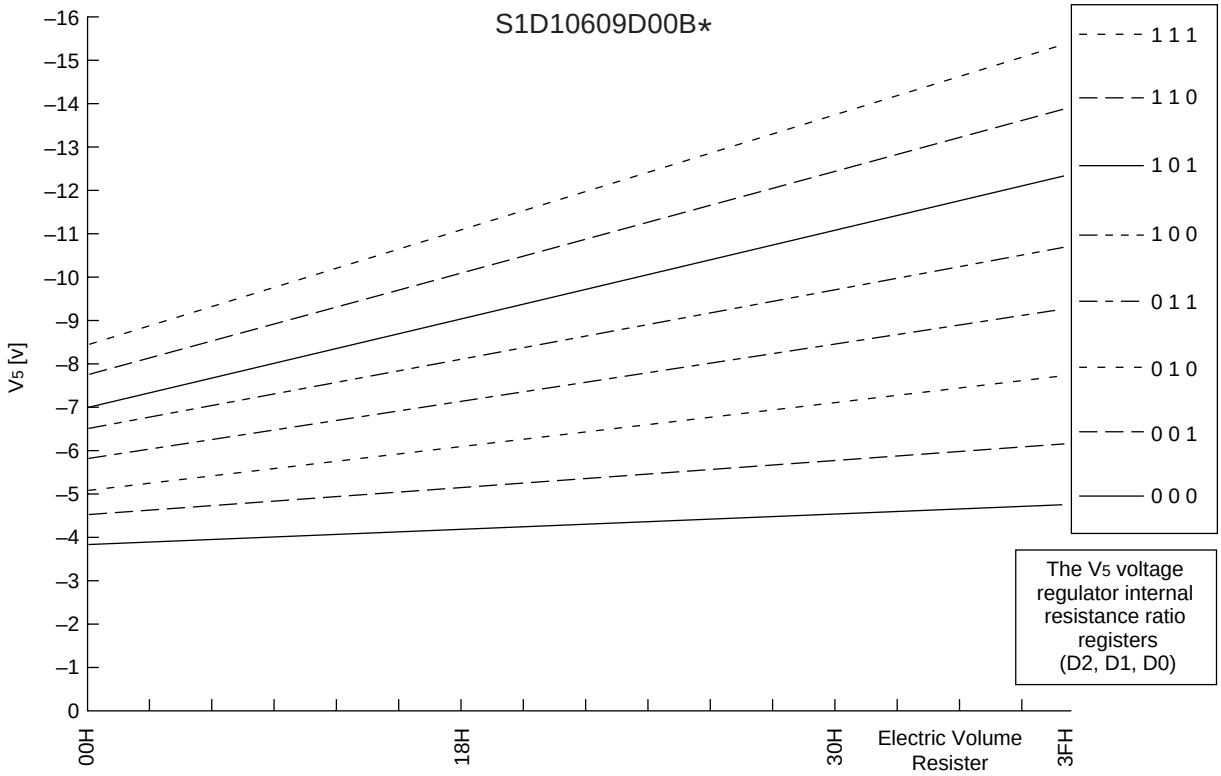


Figure 13: S1D10609D00B* Temperature Gradient = –0.05%/°C Model

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

Setup example: When selecting Ta = 25°C and V_5 = 7 V for an S1D10607 model on which Temperature gradient = –0.05%/°C.
Using Figure 15 and the equation A-1, the following setup is enabled.

Table 12

Contents	Register					
	D5	D4	D3	D2	D1	D0
For V_5 voltage regulator	—	—	—	0	1	0
Electronic Volume	1	0	0	1	0	1

At this time, the variable range and the notch width of the V_5 voltage is, as shown Table 13, as dependent on the electronic volume.

Table 13

V_5	Min.	Typ.	Max.	Units
Variable Range	–8.4 (63 levels)	–6.8 (central value)	–5.1 (0 level)	[V]
Notch width		51		[mV]

(B) When an External Resistance is Used (i.e., The V5 Voltage Regulator Internal Resistors Are Not Used) (1)

The liquid crystal power supply voltage V5 can also be set without using the V5 voltage regulator internal resistors (IRS terminal = LOW) by adding resistors Ra' and Rb' between VDD and VR, and between VR and V5, respectively. When this is done, the use of the electronic volume function makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal power supply voltage V5 through commands. In the range where | V5 | < | VOUT |, the V5 voltage can be calculated using equation B-1 based on the external resistances Ra' and Rb'.

$$V_5 = \left(1+\frac{Rb'}{Ra'}\right)\cdot V_{EV}$$
$$= \left(1+\frac{Rb'}{Ra'}\right)\cdot\left(1-\frac{\alpha}{162}\right)\cdot V_{REG}$$
$$\left[\because V_{EV} = \left(1-\alpha/162\right)\cdot V_{REG}\right] \qquad \text{(Equation B-1)}$$

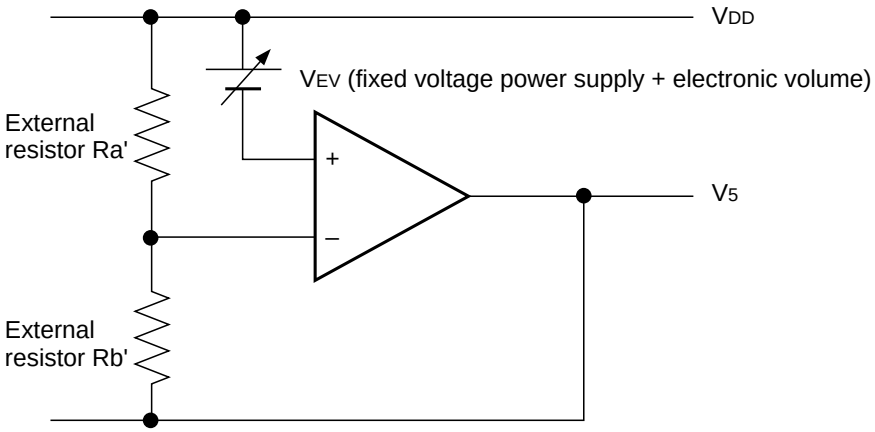


Figure 14

Setup example: When selecting Ta = 25°C and V5 = –7 V for an S1D10607 Series model where the temperature gradient = –0.05%/°C.
When the central value of the electron volume register is (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0), then α = 31 and VREG = –2.1 V so, according to equation B-1,

$$V_5 = \left(1+\frac{Rb'}{Ra'}\right)\cdot\left(1-\frac{\alpha}{162}\right)\cdot V_{REG}$$
$$-11V = \left(1+\frac{Rb'}{Ra'}\right)\cdot\left(1-\frac{31}{162}\right)\cdot(-2.1) \quad \text{(Equation B-2)}$$

Moreover, when the value of the current running through Ra' and Rb' is set to 5 μA,

$$Ra' + Rb' = 1.4M\Omega \qquad \text{(Equation B-3)}$$

Consequently, by equations B-2 and B-3,

$$\frac{Rb'}{Ra'} = 3.12$$
$$Ra' = 340k\Omega$$
$$Rb' = 1060k\Omega$$

At this time, the V5 voltage variable range and notch width, based on the electron volume function, is as given in Table 14.

Table 14

V5	Min.	Typ.	Max.	Units
Variable Range	–8.6 (63 levels)	–7.0 (central value)	–5.3 (0 level)	[V]
Notch width		52		[mV]

(C) When External Resistors are Used (i.e. The V_5 Voltage Regulator Internal Resistors Are Not Used). (2)

When the external resistor described above are used, adding a variable resistor as well makes it possible to perform fine adjustments on Ra' and Rb', to set the liquid crystal drive voltage V_5. In this case, the use of the electronic volume function makes it possible to control the liquid crystal power supply voltage V_5 by commands to adjust the liquid crystal display brightness. In the range where $|V_5| < |V_{OUT}|$ the V_5 voltage can be calculated by equation C-1 below based on the R_1 and R_2 (variable resistor) and R_3 settings, where R_2 can be subjected to fine adjustments (ΔR_2).

$$V_5 = \left(1 + \frac{R_3 + R_2 - \Delta R_2}{R_1 + \Delta R_2}\right) \cdot V_{EV}$$

$$= \left(1 + \frac{R_3 + R_2 - \Delta R_2}{R_1 + \Delta R_2}\right) \cdot \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG}$$

$$\left[\because V_{EV} = \left(1 - \alpha/162\right) \cdot V_{REG}\right] \qquad \text{(Equation C-1)}$$

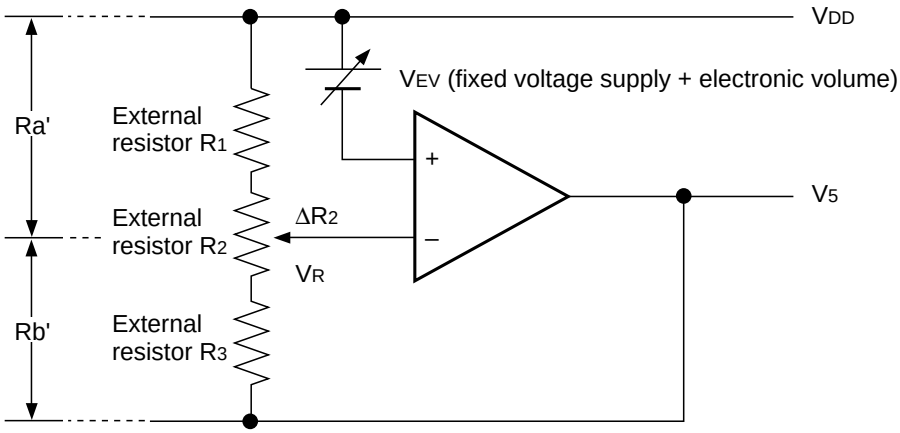


Figure 15

Setup example: When selecting Ta = 25°C and V_5 = –5 to –9 V (using R_2) for an S1D10607 model where the temperature gradient = –0.05%/°C.
When the central value for the electronic volume register is set at (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0),

$$\alpha = 31$$

$$V_{REG} = -2.1V$$

so, according to equation C-1, when $\Delta R_2 = 0\ \Omega$, in order to make V_5 = –9 V,

$$-9V = \left(1 + \frac{R_3 + R_2}{R_1}\right) \cdot \left(1 - \frac{31}{162}\right) \cdot (-2.1)$$

(Equation C-2)

When $\Delta R_2 = R_2$, in order to make V = –5 V,

$$-5V = \left(1 + \frac{R_3}{R_1 + R_2}\right) \cdot \left(1 - \frac{31}{162}\right) \cdot (-2.1)$$

(Equation C-3)

Moreover, when the current flowing V_{DD} and V_5 is set to 5 µA,

$$R_1 + R_2 + R_3 = 1.4M\Omega \qquad \text{(Equation C-4)}$$

With this, according to equation C-2, C-3 and C-4,

$$R_1 = 264k\Omega$$

$$R_2 = 211k\Omega$$

$$R_3 = 925k\Omega$$

At this time, the V_5 voltage variable range and notch width based on the electron volume function is as shown in Table 15.

Table 15

V_5	Min.	Typ.	Max.	Units
Variable Range	–8.7 (63 levels)	–7.0 (central value)	–5.3 (0 level)	[V]
Notch width		53		[mV]

* When the V_5 voltage regulator internal resistors or the electronic volume function is used, it is necessary to at least set the voltage regulator circuit and the voltage follower circuit to an operating mode using the power control set commands. Moreover, it is necessary to provide a voltage from V_{OUT} when the Booster circuit is OFF.
* The V_R terminal is enabled only when the V_5 voltage regulator internal resistors are not used (i.e. the IRS terminal = LOW). When the V_5 voltage regulator internal resistors are used (i.e. when the IRS terminal = HIGH), then the V_R terminal is left open.
* Because the input impedance of the V_R terminal is high, it is necessary to take into consideration short leads, shield cables, etc. to handle noise.

The Liquid Crystal Voltage Generator Circuit

The V_5 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V_1, V_2, V_3, and V_4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V_1, V_2, V_3 and V_4 to the liquid crystal drive circuit. 1/9 bias or 1/7 bias for S1D10605 Series, 1/8 bias or 1/6 bias for S1D10606 Series, 1/6 bias or 1/5 bias for the S1D10607 Series 1/8 bias or 1/6 bias for S1D10608 Series and 1/8 bias or 1/6 bias for S1D10609 Series can be selected.

High Power Mode

The power supply circuit equipped in the S1D10605 Series chips has very low power consumption (normal mode: $\overline{HPM}$ = HIGH). However, for LCDs or panels with large loads, this low-power power supply may cause display quality to degrade. When this occurs, setting the $\overline{HPM}$ terminal to LOW (high power mode) can improve the quality of the display. We recommend that the display be checked on actual equipment to determine whether or not to use this mode.
Moreover, if the improvement to the display is inadequate even after high power mode has been set, then it is necessary to add a liquid crystal drive power supply externally.

The Internal Power Supply Shutdown Command Sequence

The sequence shown in Figure 16 is recommended for shutting down the internal power supply, first placing the power supply in power saver mode and then turning the power supply OFF.

Sequence	Details (Command, status)	Command address D7	D6	D5	D4	D3	D2	D1	D0	
Step1	Display OFF	1	0	1	0	1	1	1	0	Power saver commands (compound)
⬇										
Step2	Display all points ON	1	0	1	0	0	1	0	1	
⬇										
End	Internal power supply OFF									

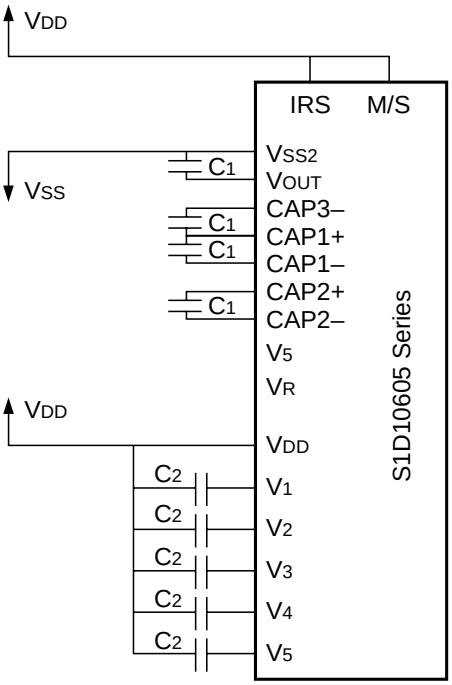
Figure 16

Reference Circuit Examples

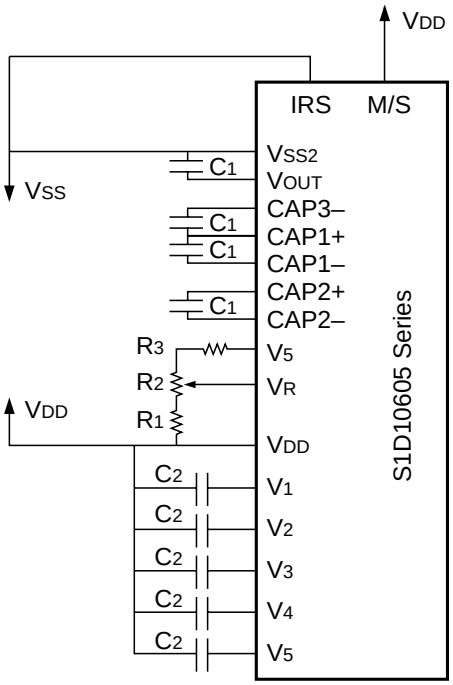
Figure 17 shows reference circuit examples.

① When used all of the step-up circuit, voltage regulating circuit and V/F circuit

(1) When the voltage regulator internal resistor is used.
(Example where $V_{SS2} = V_{SS}$, with 4x step-up)

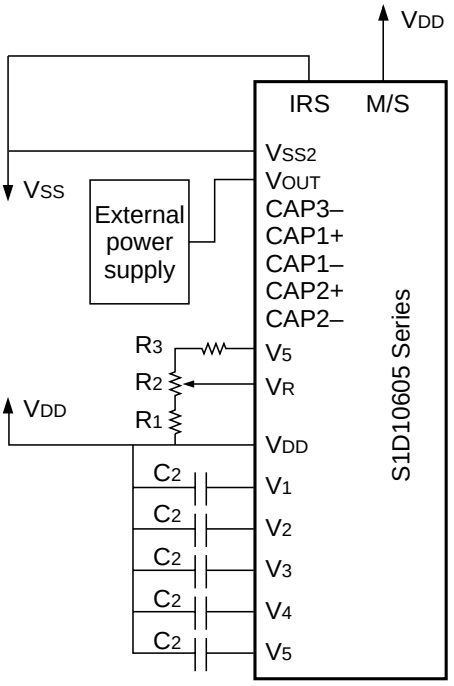


(2) When the voltage regulator internal resistor is not used.
(Example where $V_{SS2} = V_{SS}$, with 4x step-up)

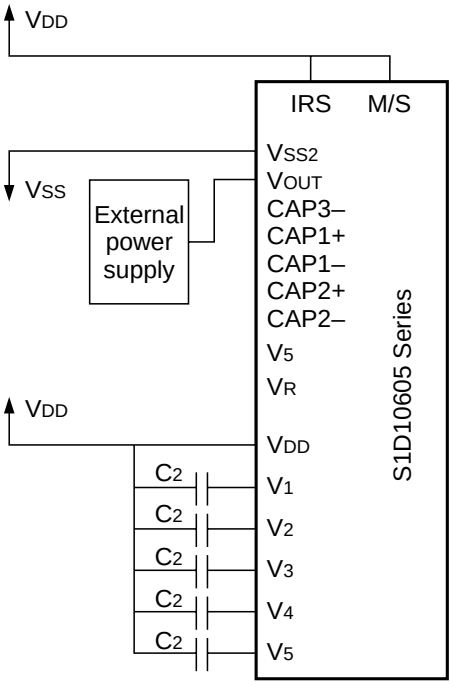


② When the voltage regulator circuit and V/F circuit alone are used

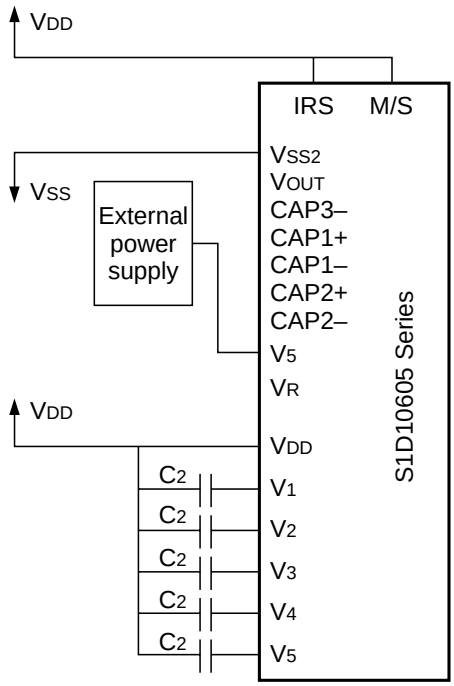
(1) When the V_5 voltage regulator internal resistor is not used.



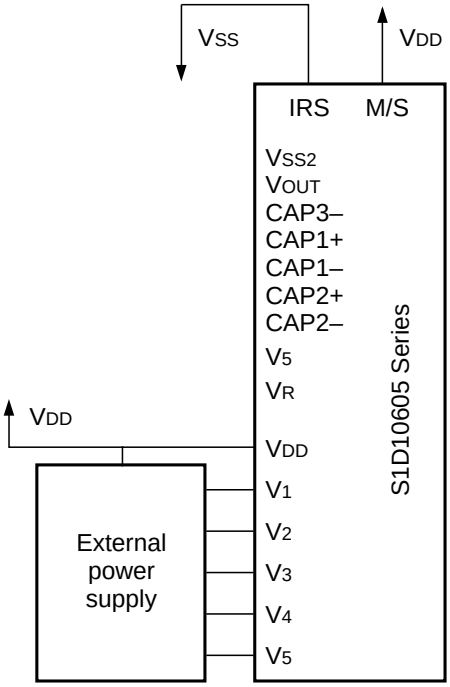
(2) When the V_5 voltage regulator internal resistor is used.



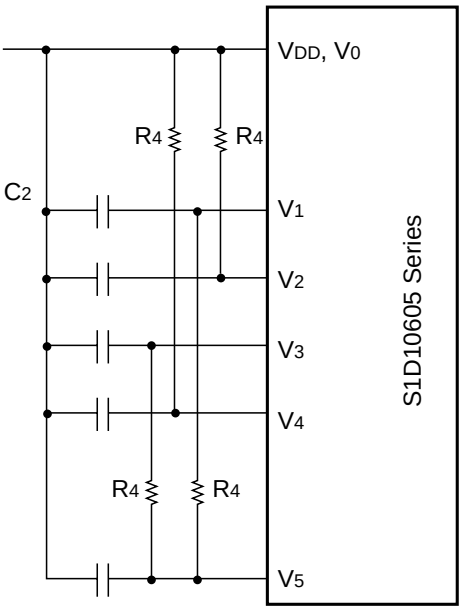
③ When the V/F circuit alone is used



④ When the built-in power is not used



⑤ When the built-in power circuit is used to drive a liquid crystal panel heavily loaded with AC or DC, it is recommended to connect an external resistor to stabilize potentials of V_1, V_2, V_3 and V_4 which are output from the built-in voltage follower.



Examples of shared reference settings
When V_5 can vary between –8 and 12 V

Item	Set value	Units
C_1	1.0 to 4.7	µF
C_2	0.01 to 1.0	µF

Reference set value R_4: 100KΩ to 1MΩ
It is recommended to set an optimum resistance value R_4 taking the liquid crystal display and the drive waveform.

Figure 17

* 1 Because the V_R terminal input impedance is high, use short leads and shielded lines.
* 2 C_1 and C_2 are determined by the size of the LCD being driven. Select a value that will stabilize the liquid crystal drive voltage.

Example of the Process by which to Determine the Settings:

- Turn the voltage regulator circuit and voltage follower circuit ON and supply a voltage to V_{OUT} from the outside.
- Determine C_2 by displaying an LCD pattern with a heavy load (such as horizontal stripes) and selecting a C_2 that stabilizes the liquid crystal drive voltages (V_1 to V_5). Note that all C_2 capacitors must have the same capacitance value.
- Next turn all the power supplies ON and determine C_1.

* Precautions when installing the COG

When installing the COG, it is necessary to duly consider the fact that there exists a resistance of the ITO wiring occurring between the driver chip and the externally connected parts (such as capacitors and resistors). By the influence of this resistance, non-conformity may occur with the indications on the liquid crystal display.
Therefore, when installing the COG design the module paying sufficient considerations to the following three points.

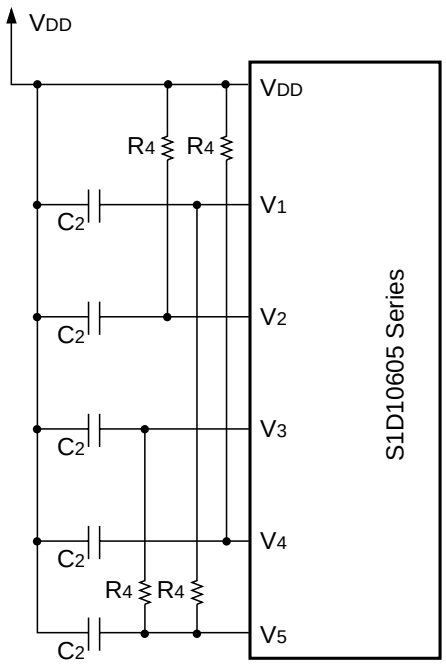
1. Suppress the resistance occurring between the driver chip pin to the externally connected parts as much as possible.
2. Suppress the resistance connecting to the power supply pin of the driver chip.
3. Make various COG module samples with different ITO sheet resistance to select the module with the sheet resistance with sufficient operation margin.

Also, as for this driver IC, pay sufficient attention to the following points when connecting to external parts for the characteristics of the circuit.

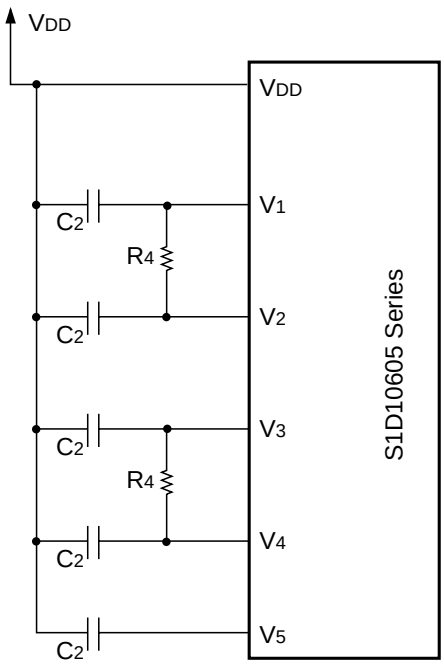
1. Connection to the boosting capacitors The boosting capacitors (the capacitors connecting to respective CAP pins and capacitor being inserted between V_{OUT} and V_{SS2}) of this IC are being switched over by use of the transistor with very low ON-resistance of about 10Ω. However, when installing the COG, the resistance of ITO wiring is being inserted in series with the switching transistor, thus dominating the boosting ability.
   Consequently, the boosting ability will be hindered as a result and pay sufficient attention to the wiring to respective boosting capacitors.
2. Connection of the smoothing capacitors for the liquid crystal drive
   The smoothing capacitors for the liquid crystal driving potentials (V_1. V_2, V_3 and V_4) are indispensable for liquid crystal drives not only for the purpose of mere stabilization of the voltage levels. If the ITO wiring resistance which occurs pursuant to installation of the COG is supplemented to these smoothing capacitors, the liquid crystal driving potentials become unstable to cause non-conformity with the indications of the liquid crystal display. Therefore, when using the COG module, we definitely recommend to connect reinforcing resistors externally.
   Reference value of the resistance is 100kΩ to 1MΩ. Meanwhile, because of the existence of these reinforcing resistors, current consumption will increase.

Indicated below is an exemplary connection diagram of external resistors.
Please make sufficient evaluation work for the display statuses with any connection tests.

Exemplary connection diagram 1.



Exemplary connection diagram 2.



The Reset Circuit

When the $\overline{RES}$ input comes to the LOW level, these LSIs return to the default state. Their default states are as follows:

1. Display OFF
2. Normal display
3. ADC select: Normal (ADC command D0 = LOW)
4. Power control register: (D2, D1, D0) = (0, 0, 0)
5. Serial interface internal register data clear
6. LCD power supply bias rate:
   S1D10605***** ..... 1/9 bias
   S1D10606*****, 10608*****,
   10609***** ..... 1/8 bias
   S1D10607***** ..... 1/6 bias
7. All-indicator lamps-on OFF (All-indicator lamps ON/OFF command D0 = LOW)
8. Power saving clear
9. V_5 voltage regulator internal resistors Ra and Rb separation
   (Internal resistors are connected while $\overline{RES}$ is LOW.)
10. Output conditions of SEG and COM terminals
    SEG : V_2/V_3, COM : V_1/V_4
    (Both the SEG terminal and the COM terminal output the VDA level while $\overline{RES}$ is LOW.)
11. Read modify write OFF
12. Static indicator OFF
    Static indicator register : (D1, D2) = (0, 0)
13. Display start line set to first line
14. Column address set to Address 0
15. Page address set to Page 0
16. Common output status normal
17. V_5 voltage regulator internal resistor ratio set mode clear
18. Electronic volume register set mode clear
    Electronic volume register : (D5, D4, D3, D2, D1, D0) = (1, 0. 0, 0, 0, 0)
19. Test mode clear

On the other hand, when the reset command is used, the above default settings from 11 to 19 are only executed.

When the power is turned on, the IC internal state becomes unstable, and it is necessary to initialize it using the $\overline{RES}$ terminal. After the initialization, each input terminal should be controlled normally.
Moreover, when the control signal from the MPU is in the high impedance, an overcurrent may flow to the IC. After applying a current, it is necessary to take proper measures to prevent the input terminal from getting into the high impedance state.
If the internal liquid crystal power supply circuit is not used, it is necessary that $\overline{RES}$ is HIGH when the external liquid crystal power supply is turned on. This IC has the function to discharge V_5 when $\overline{RES}$ is LOW, and the external power supply short-circuits to V_{DD} when $\overline{RES}$ is LOW.
While $\overline{RES}$ is LOW, the oscillator and the display timing generator stop, and the CL, FR, FRS and $\overline{DOF}$ terminals are fixed to HIGH. The terminals D0 to D7 are not affected. The V_{DD} level is output from the SEG and COM output terminals. This means that an internal resistor is connected between V_{DD} and V_5.

8. COMMAND DESCRIPTION

The S1D10605 Series chips identify the data bus signals by a combination of A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$) signals. Command interpretation and execution does not depend on the external clock, but rather is performed through internal timing only, and thus the processing is fast enough that normally a busy check is not required.
In the 8080 MPU interface, commands are launched by inputting a low pulse to the $\overline{RD}$ terminal for reading, and inputting a low pulse to the $\overline{WR}$ terminal for writing. In the 6800 Series MPU interface, the interface is placed in a read mode when an HIGH signal is input to the R/$\overline{W}$ terminal and placed in a write mode when a LOW signal is input to the R/$\overline{W}$ terminal and then the command is launched by inputting a high pulse to the E terminal. (See "11. Timing Characteristics" regarding the timing.) Consequently, the 6800 Series MPU interface is different than the 80x86 Series MPU interface in that in the explanation of commands and the display commands the status read and display data read $\overline{RD}$ (E) becomes "1(H)". In the explanations below the commands are explained using the 8080 Series MPU interface as the example.
When the serial interface is selected, the data is input in sequence starting with D7.
<Explanation of Commands>

(1) Display ON/OFF

This command turns the display ON and OFF.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1	Display ON
										0	Display OFF

When the display OFF command is executed when in the display all points ON mode, power saver mode is entered. See the section on the (20) "power saver" for details.

(2) Display Start Line Set

This command is used to specify the display start line address of the display data RAM shown in Figure 4. For further details see the 7. FUNCTION DESCRIPTION in "The Line Address Circuit".

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					0	0	0	0	1	0	2
								↓			↓
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

(3) Page Address Set

This command specifies the page address corresponding to the low address when the MPU accesses the display data RAM (see Figure 4). Specifying the page address and column address enables to access a desired bit of the display data RAM. Changing the page address does not accompany a change in the status display. See the "page address" circuit in the 7. Function Description for the detail.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							0	0	1	0	2
									↓		↓
							0	1	1	1	7
							1	0	0	0	8

(4) Column Address Set

This command specifies the column address of the display data RAM shown in Figure 4. The column address is split into two sections (the higher 4 bits and the lower 4 bits) when it is set (fundamentally, set continuously). Each time the display data RAM is accessed, the column address automatically increments (+1), making it possible for the MPU to continuously read from/write to the display data. The column address increment is topped at 83H. This does not change the page address continuously. See the 7. Function Description in "The Column Address Circuit," for details.

	A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	A7	A6	A5	A4	A3	A2	A1	A0	Column address
High bits →	0	1	0	0	0	0	1	A7	A6	A5	A4	0	0	0	0	0	0	0	0	0
Low bits →							0	A3	A2	A1	A0	0	0	0	0	0	0	0	1	1
												0	0	0	0	0	0	1	0	2
																↓				↓
												1	0	0	0	0	0	1	0	130
												1	0	0	0	0	0	1	1	131

(5) Status Read

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY	When BUSY = 1, it indicates that either processing is occurring internally or a reset condition is in process. While the chip does not accept commands until BUSY = 0, if the cycle time can be satisfied, there is no need to check for BUSY conditions.
ADC	This shows the relationship between the column address and the segment driver. 0: Reverse (column address 131-n ↔ SEG n) 1: Normal (column address n ↔ SEG n) (The ADC command switches the polarity.)
ON/OFF	ON/OFF: indicates the display ON/OFF state. 0: Display ON 1: Display OFF (This display ON/OFF command switches the polarity.)
RESET	This indicates that the chip is in the process of initialization either because of a $\overline{RES}$ signal or because of a reset command. 0: Operating state 1: Reset in progress

(6) Display Data Write

This command writes 8-bit data to the specified display data RAM address. Since the column address is automatically incremented by "1" after the write, the MPU can write the display data.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

(7) Display Data Read

This command reads 8-bit data from the specified display data RAM address. Since the column address is automatically incremented by "1" after the read, the CPU can continuously read multiple-word data. One dummy read is required immediately after the column address has been set. See the 7. Function Description in "Display Data RAM" for the explanation of accessing the internal registers. When the serial interface is used, reading of the display data becomes unavailable.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read Data							

(8) ADC Select (Segment Driver Direction Select)

This command can reverse the correspondence between the display RAM data column address and the segment driver output. Thus, sequence of the segment driver output pins may be reversed by the command. See the 7. Function Description "column address circuit" for the detail. Increment of the column address (by "1") accompanying the reading or writing the display data is done according to the column address indicated in Figure 4.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

(9) Display Normal/Reverse

This command can reverse the lit and unlit display without overwriting the contents of the display data RAM. When this is done the display data RAM contents are maintained.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	RAM Data HIGH LCD ON voltage (normal)
										1	RAM Data LOW LCD ON voltage (reverse)

(10) Display All Points ON/OFF

This command makes it possible to force all display points ON regardless of the content of the display data RAM. The contents of the display data RAM are maintained when this is done. This command takes priority over the display normal/reverse command.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display mode
										1	Display all points ON

When the display is in an OFF mode, executing the display all points ON command will place the display in power save mode. For details, see the (20) "Power Save section".

(11) LCD Bias Set

This command selects the voltage bias ratio required for the liquid crystal display.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Select Status S1D10605*****	S1D10606*****	S1D10607*****	S1D10608*****	S1D10609*****
0	1	0	1	0	1	0	0	0	1	0	1/9 bias	1/8 bias	1/6 bias	1/8 bias	1/8 bias
										1	1/7 bias	1/6 bias	1/5 bias	1/6 bias	1/6 bias

(12) Read/Modify/Write

This command is used paired with the "END" command. Once this command has been input, the display data read command does not change the column address, but only the display data write command increments (+1) the column address. This mode is maintained until the END command is input. When the END command is input, the column address returns to the address it was at when the read/modify/write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

* Even in read/modify/write mode, other commands aside from display data read/write commands can also be used. However, the column address set command cannot be used.

- The sequence for cursor display

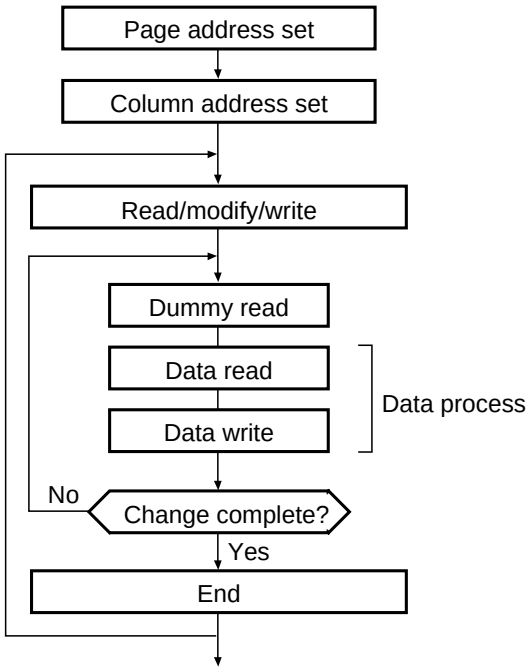


Figure 18

(13) End

This command releases the read/modify/write mode, and returns the column address to the address it was at when the mode was entered.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

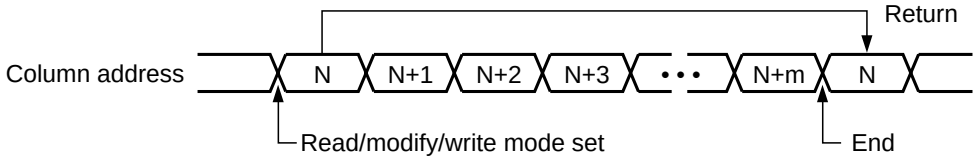


Figure 19

(14) Reset

This command initializes the display start line, the column address, the page address, the common output mode, the V_5 voltage regulator internal resistor ratio, the electronic volume, and the static indicator are reset, and the read/modify/write mode and test mode are released. There is no impact on the display data RAM. See the 7. Function Description in “Reset” for details.
The reset operation is performed after the reset command is entered.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The initialization when the power supply is applied must be done through applying a reset signal to the $\overline{RES}$ terminal. The reset command must not be used instead.

(15) Common Output Mode Select

This command can select the scan direction of the COM output terminal. For details, see the 7. Function Description in "Common Output Mode Select Circuit."

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0		Selected Mode				
												S1D10605*****	S1D10606*****	S1D10607*****	S1D10608*****	S1D10609*****
0	1	0	1	1	0	0	0	*	*	*	Normal	COM0→COM63	COM0→COM47	COM0→COM31	COM0→COM53	COM0→COM51
							1				Reverse	COM63→COM0	COM47→COM0	COM31→COM0	COM53→COM0	COM51→COM0

* Disabled bit

(16) Power Controller Set

This command sets the power supply circuit functions. See the 7. Function Description in "The Power Supply Circuit," for details

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode
0	1	0	0	0	1	0	1	0			Booster circuit: OFF
								1			Booster circuit: ON
									0		Voltage regulator circuit: OFF
									1		Voltage regulator circuit: ON
										0	Voltage follower circuit: OFF
										1	Voltage follower circuit: ON

[Translator's Note: the abbreviations explained within these parentheses for V and V/F have been written out in the English translation and are therefore no longer necessary.]

(17) V_5 Voltage Regulator Internal Resistor Ratio Set

This command sets the V_5 voltage regulator internal resistor ratio. For details, see the 7. Function Description is "The Power Supply Circuits."

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Rb/Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
									↓		↓
								1	1	0	
								1	1	1	Large

(18) The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal drive voltage V_5 through the output from the voltage regulator circuits of the internal liquid crystal power supply. This command is a two byte command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

• The Electronic Volume Mode Set

When this command is input, the electronic volume register set command becomes enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

• Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal drive voltage V_5 assumes one of the 64 voltage levels.
When this command is input, the electronic volume mode is released after the electronic volume register has been set.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	| V5 |
0	1	0	*	*	0	0	0	0	0	1	Small
0	1	0	*	*	0	0	0	0	1	0	
0	1	0	*	*	0	0	0	0	1	1	
						↓					↓
0	1	0	*	*	1	1	1	1	1	0	
0	1	0	*	*	1	1	1	1	1	1	Large

* Inactive bit

When the electronic volume function is not used, set this to (1, 0, 0, 0, 0, 0)

• The Electronic Volume Register Set Sequence

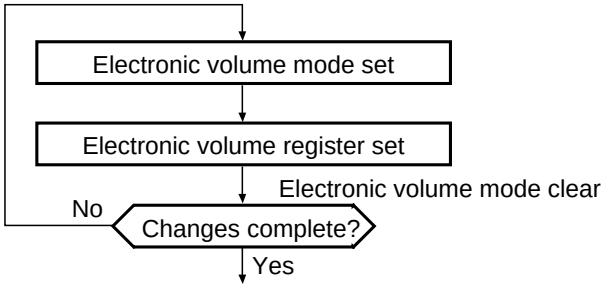


Figure 20

(19) Static Indicator (Double Byte Command)

This command controls the static drive system indicator display. The static indicator display is controlled by this command only, and is independent of other display control commands.
This is used when one of the static indicator liquid crystal drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal. A different pattern is recommended for the static indicator electrodes than for the dynamic drive electrodes. If the pattern is too close, it can result in deterioration of the liquid crystal and of the electrodes.
The static indicator ON command is a double byte command paired with the static indicator register set command, and thus one must execute one after the other. (The static indicator OFF command is a single byte command.)

• Static Indicator ON/OFF

When the static indicator ON command is entered, the static indicator register set command is enabled. Once the static indicator ON command has been entered, no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Static Indicator
0	1	0	1	0	1	0	1	1	0	0	OFF
										1	ON

• Static Indicator Register Set

This command sets two bits of data into the static indicator register, and is used to set the static indicator into a blinking mode.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Indicator Display State
0	1	0	*	*	*	*	*	*	0	0	OFF
									0	1	ON (blinking at approximately one second intervals)
									1	0	ON (blinking at approximately 0.5 second intervals)
									1	1	ON (constantly on)

* Disabled bit

• Static Indicator Register Set Sequence

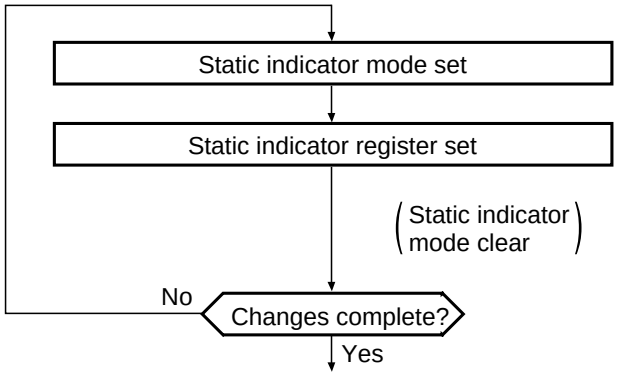


Figure 21

(20) Power Save (Compound Command)

When the display all points ON is performed while the display is in the OFF mode, the power saver mode is entered, thus greatly reducing power consumption.
The power saver mode has two different modes: the sleep mode and the standby mode. When the static indicator is OFF, it is the sleep mode that is entered. When the static indicator is ON, it is the standby mode that is entered.
In the sleep mode and in the standby mode, the display data is saved as is the operating mode that was in effect before the power saver mode was initiated, and the MPU is still able to access the display data RAM.
Refer to figure 22 for power save off sequence.

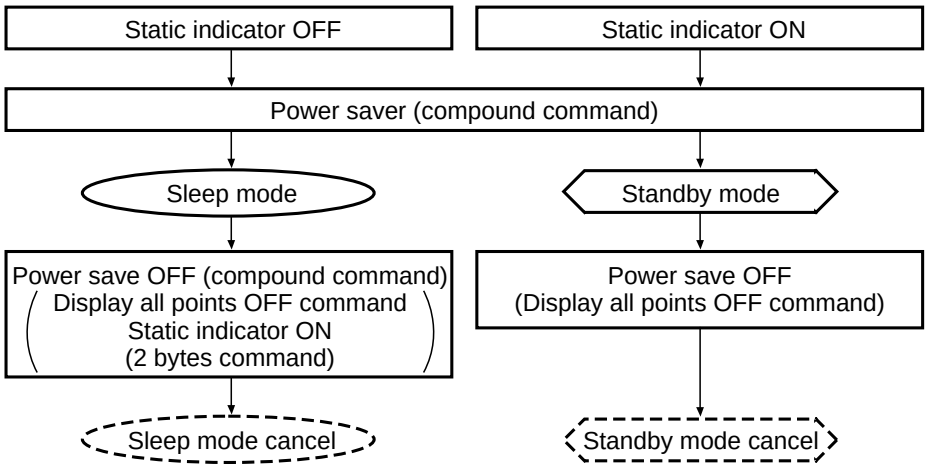


Figure 22

• Sleep Mode

This stops all operations in the LCD display system, and as long as there are no accesses from the MPU, the consumption current is reduced to a value near the static current. The internal modes during sleep mode are as follows:

① The oscillator circuit and the LCD power supply circuit are halted.
② All liquid crystal drive circuits are halted, and the segment in common drive outputs output a V_{DD} level.

• Standby Mode

The duty LCD display system operations are halted and only the static drive system for the indicator continues to operate, providing the minimum required consumption current for the static drive. The internal modes are in the following states during standby mode.

① The LCD power supply circuits are halted. The oscillator circuit continues to operate.
② The duty drive system liquid crystal drive circuits are halted and the segment and common driver outputs output a V_{DD} level. The static drive system does not operate.

When a reset command is performed while in standby mode, the system enters sleep mode.

* When an external power supply is used, it is recommended that the functions of the external power supply circuit be stopped when the power saver mode is started. For example, when the various levels of liquid crystal drive voltage are provided by external resistive voltage dividers, it is recommended that a circuit be added in order to cut the electrical current flowing through the resistive voltage divider circuit when the power saver mode is in effect. The S1D10605 series chips have a liquid crystal display blanking control terminal $\overline{DOF}$. This terminal enters an LOW state when the power saver mode is launched. Using the output of $\overline{DOF}$, it is possible to stop the function of an external power supply circuit.
* When the master is turned on, the oscillator circuit is operable immediately after the powering on.

(21) NOP

Non-OPeration Command

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

(22) Test

This is a command for IC chip testing. Please do not use it. If the test command is used by accident, it can be cleared by applying a LOW signal to the RES input by the reset command or by using an NOP.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	*	*	*	*

* Inactive bit

Note: The S1D10605 Series chips maintain their operating modes until something happens to change them. Consequently, excessive external noise, etc., can change the internal modes of the S1D10605 Series chip. Thus in the packaging and system design it is necessary to suppress the noise or take measure to prevent the noise from influencing the chip. Moreover, it is recommended that the operating modes be refreshed periodically to prevent the effects of unanticipated noise.

Table 16 Table of S1D10605 Series Commands

	Command	Command Code											Function
		A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2)	Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3)	Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4)	Column address set upper bit	0	1	0	0	0	0	1	Most significant column address				Sets the most significant 4 bits of the display RAM column address.
	Column address set lower bit	0	1	0	0	0	0	0	Least significant column address				Sets the least significant 4 bits of the display RAM column address.
(5)	Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6)	Display data write	1	1	0	Write data								Writes to the display RAM
(7)	Display data read	1	0	1	Read data								Reads from the display RAM
(8)	ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9)	Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10)	Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11)	LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio S1D10605***** .... 0: 1/9, 1: 1/7 S1D10606***** /S1D10608***** /S1D10609***** ... 0: 1/8, 1: 1/6 S1D10607***** 0: 1/6, 1: 1/5
(12)	Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13)	End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14)	Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15)	Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction, 1: reverse direction
(16)	Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17)	V_5 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio (Rb/Ra) mode
(18)	Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1	
	Electronic volume register set	0	1	0	*	*	Electronic volume value						Set the V_5 output voltage electronic volume register
(19)	Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0 1	0: OFF, 1: ON
	Static indicator register set	0	1	0	*	*	*	*	*	*	Mode		Set the flashing mode
(20)	Power saver												Display OFF and display all points ON compound command
(21)	NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(22)	Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

(Note) *: disabled data

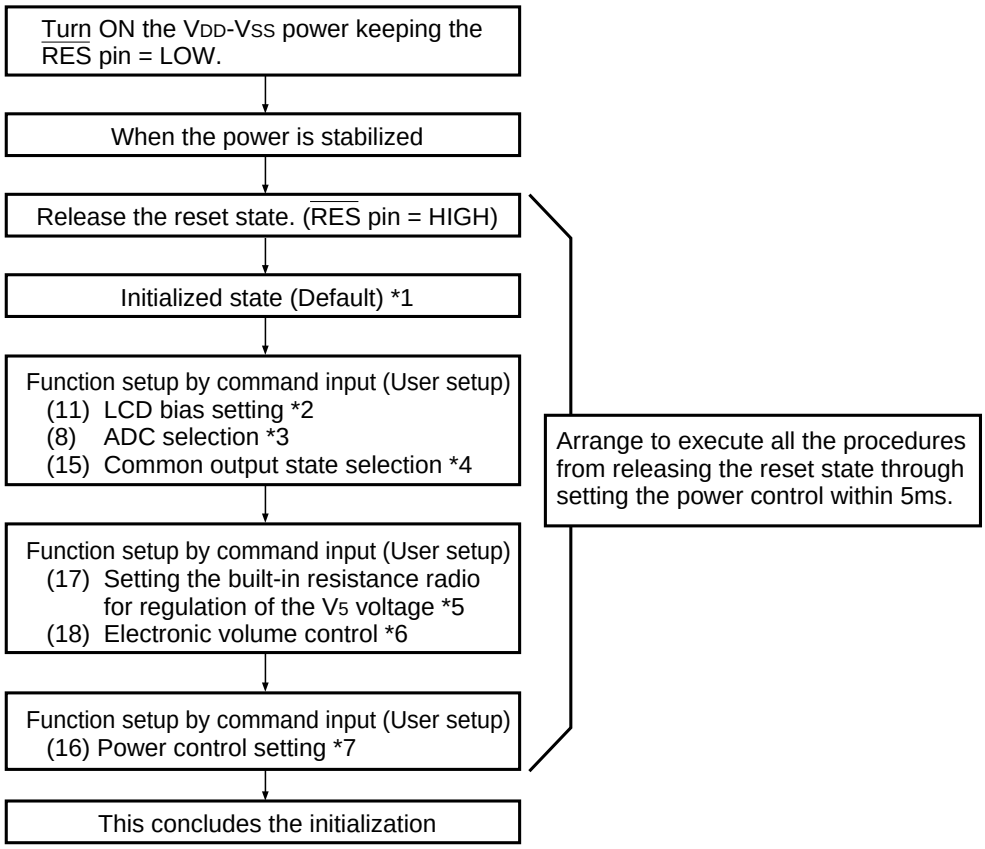
9. COMMAND DESCRIPTION

Instruction Setup: Reference (reference)

(1) Initialization

Note: With this IC, when the power is applied, LCD driving non-selective potentials V_2 and V_3 (SEG pin) and V_1 and V_4 (COM pin) are output through the LCD driving output pins SEG and COM. When electric charge is remaining in the smoothing capacitor connecting between the LCD driving voltage output pins (V_1 to V_5) and the V_{DD} pin, the picture on the display may become totally dark instantaneously when the power is turned on. To avoid occurrence of such a failure, we recommend the following flow when turning on the power.

① When the built-in power is being used immediately after turning on the power:

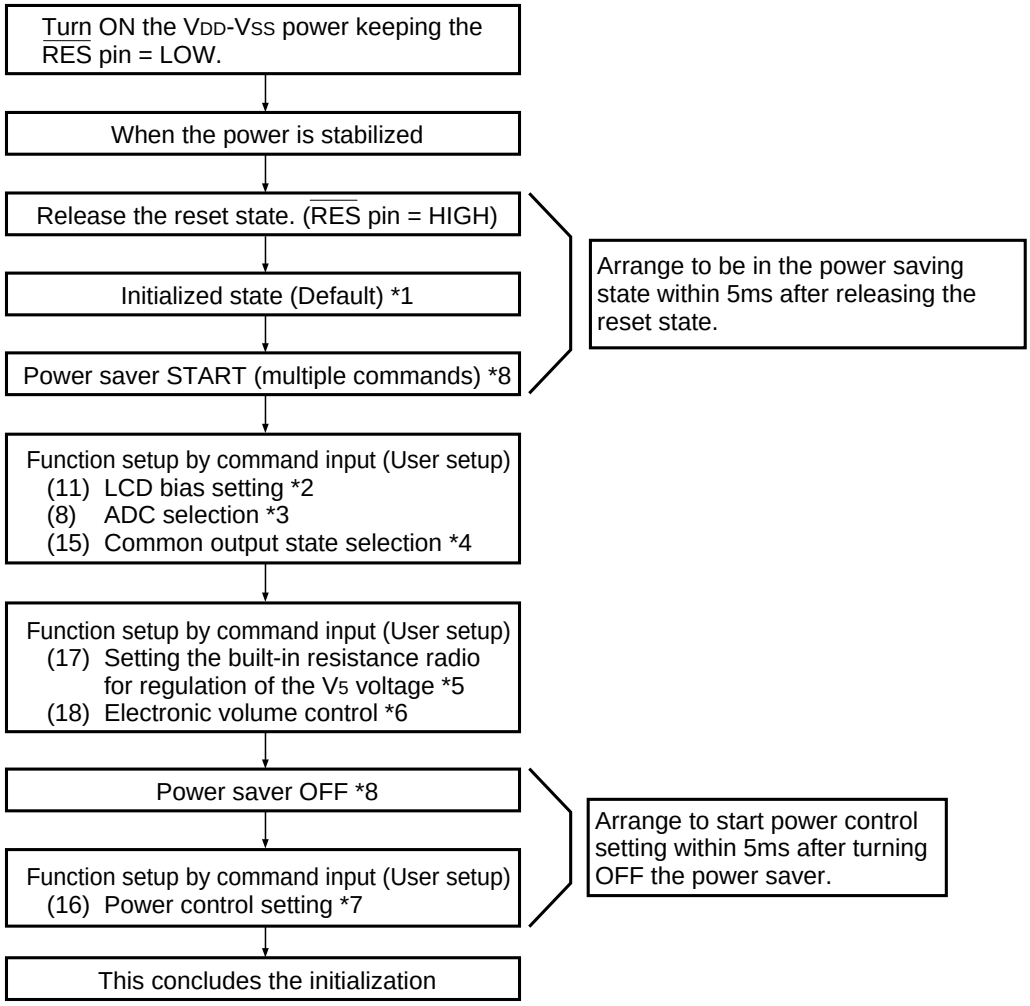


* The target time of 5ms will result to vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

Notes: Refer to respective sections or paragraphs listed below.

*1: 7. Function description; “Resetting circuit”
*2: 8. Command description; (11) “LCD bias setting”
*3: 8. Command description; (8) “ADC selection”
*4: 8. Command description; (15) “Common output state selection”
*5: 7. Function description of functions; “Power circuit” & 8. Command description; (17) “Setting the built-in resistance radio for regulation of the V_5 voltage”
*6: 7. Function description; “Power circuit” & 8. Command description; (18) “Electronic volume control”
*7: 7. Function description; “Power circuit” & 8. Command description; (16) “Power control setting”

② When the built-in power is not being used immediately after turning on the power:

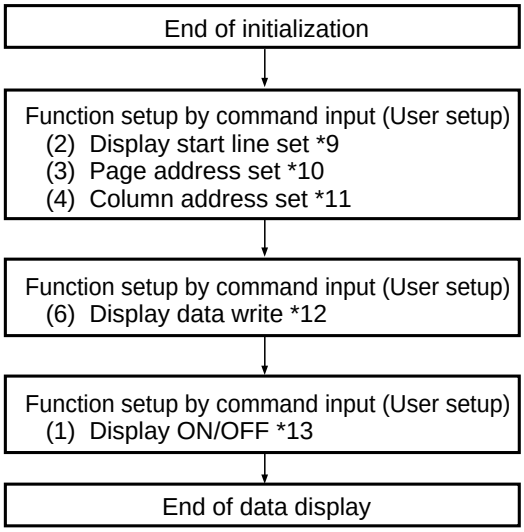


* The target time of 5ms will result to vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

Notes: Refer to respective sections or paragraphs listed below.

*1: 7. Function description; “Resetting circuit”
*2: 8. Command description; (11) “LCD bias setting”
*3: 8. Command description; (8) “ADC selection”
*4: 8. Command description; (15) “Common output state selection”
*5: 7. Function description; “Power circuit” & 8. Command description; “Setting the built-in resistance radio for regulation of the V5 voltage”
*6: 7. Function description; “Power circuit” & 8. Command description; “Electronic volume control”
*7: 7. Function description; “Power circuit” & 8. Command description; “Power control setting”
*8: The power saver ON state can either be in sleep state or stand-by state.
8. Command description; Power saver START (multiple commands)

(2) Data Display



Notes: Reference items

*9: 8. Command Description; (2) "Display start line set"

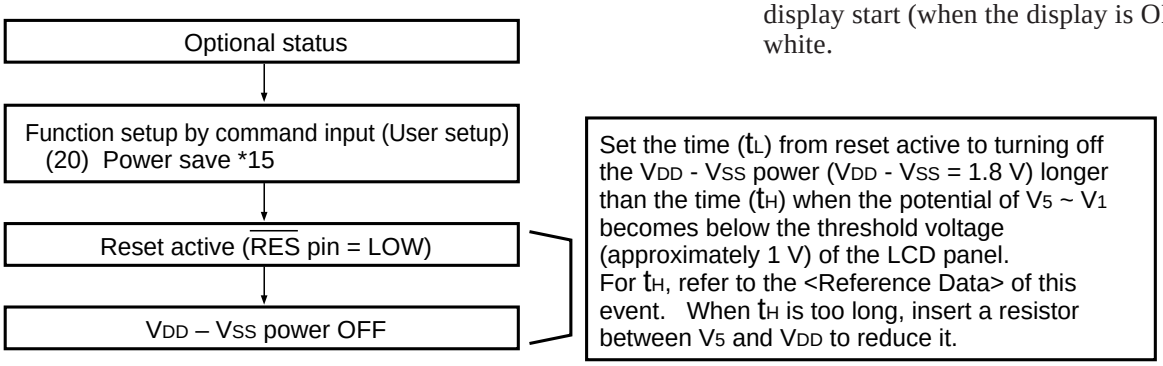
*10: 8. Command Description; (3) "Page address set"

*11: 8. Command Description; (4) "Column address set"

*12: 8. Command Description; (6) "Display data write"

*13: 8. Command Description; (1) "Display ON/OFF"
Avoid displaying all the data at the data display start (when the display is ON) in white.

(3) Power OFF *14



Notes: Reference items

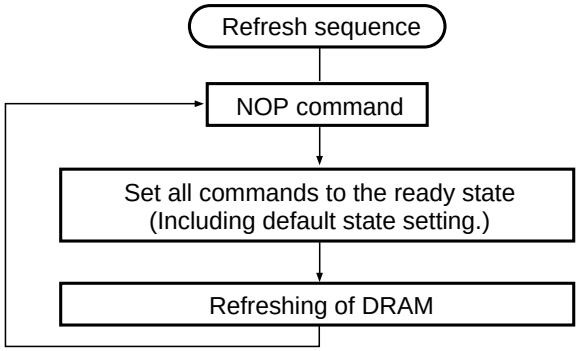
*14: The logic circuit of this IC's power supply V_{DD} - V_{SS} controls the driver of the LCD power supply V_{DD} - V_5. So, if the power supply V_{DD} - V_{SS} is cut off when the LCD power supply V_{DD} - V_5 has still any residual voltage, the driver (COM. SEG) may output any uncontrolled voltage. When turning off the power, observe the following basic procedures:

- After turning off the internal power supply, make sure that the potential V_5 to V_1 has become below the threshold voltage of the LCD panel, and then turn off this IC's power supply (V_{DD} - V_{SS}).
  6. Description of Function, 6.7 Power Circuit

*15: After inputting the power save command, be sure to reset the function using the $\overline{RES}$ terminal until the power supply V_{DD} - V_{SS} is turned off. 7. Command Description (20) "Power Save"

Refresh

It is recommended that the operating modes and display contents be refreshed periodically to prevent the effect of unexpected noise.

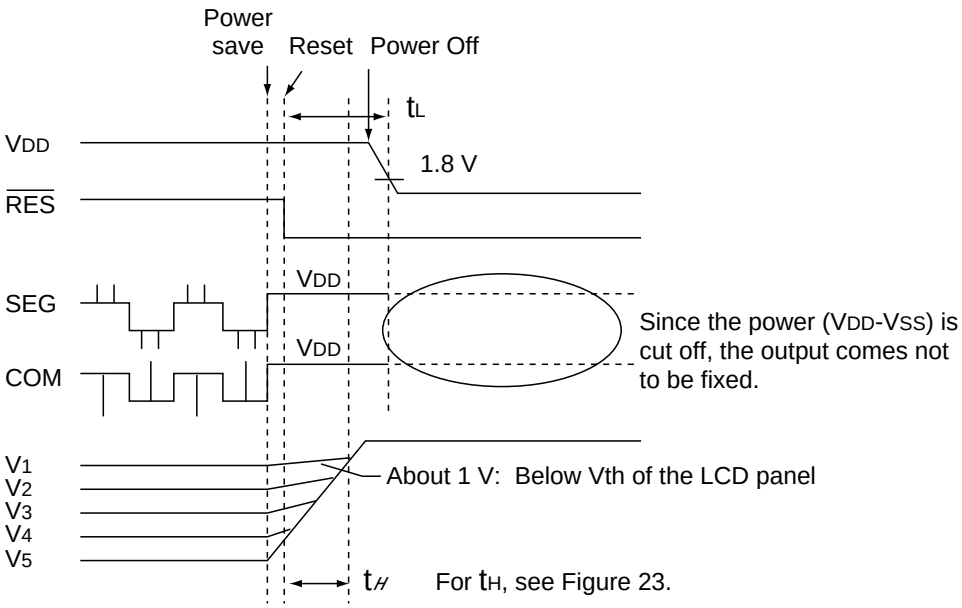


Precautions on Turning off the power

Observe Paragraph 1) as the basic rule.

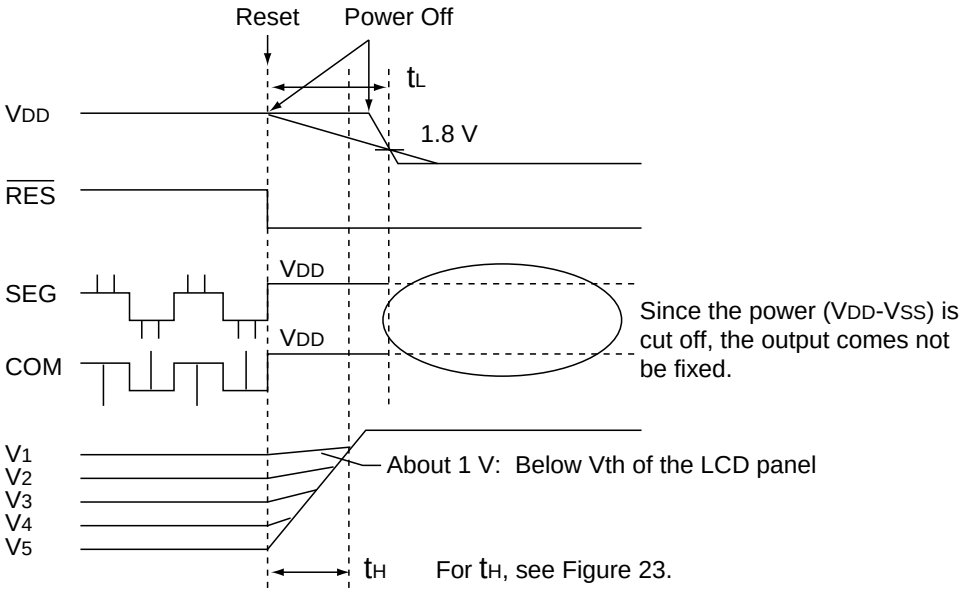
<Turning the power (V_{DD} - V_{SS}) off>

1) Power Save (The LCD powers (V_{DD} - V_5) are off.) → Reset input → Power (V_{DD} - V_{SS}) OFF
   - Observe $t_L > t_H$.
   - When $t_L < t_H$, an irregular display may occur.
     Set t_L on the MPU according to the software. t_H is determined according to the external capacity C_2 (smoothing capacity of V_5 to V_1) and the driver's discharging capacity.



<Turning the power (V_{DD} - V_{SS}) off : When command control is not possible.>

2) Reset (The LCD powers (V_{DD} - V_{SS}) are off.) → Power (V_{DD} - V_{SS}) OFF
   - Observe $t_L > t_H$.
   - When $t_L < t_H$, an irregular display may occur.
     For t_L, make the power (V_{DD} - V_{SS}) falling characteristics longer or consider any other method. t_H is determined according to the external capacity C_2 (smoothing capacity of V_5 to V_1) and the driver's discharging capacity.



<Reference Data>

V_5 voltage falling (discharge) time (t_H) after the process of operation → power save → reset.
V_5 voltage falling (discharge) time (t_H) after the process of operation → reset.

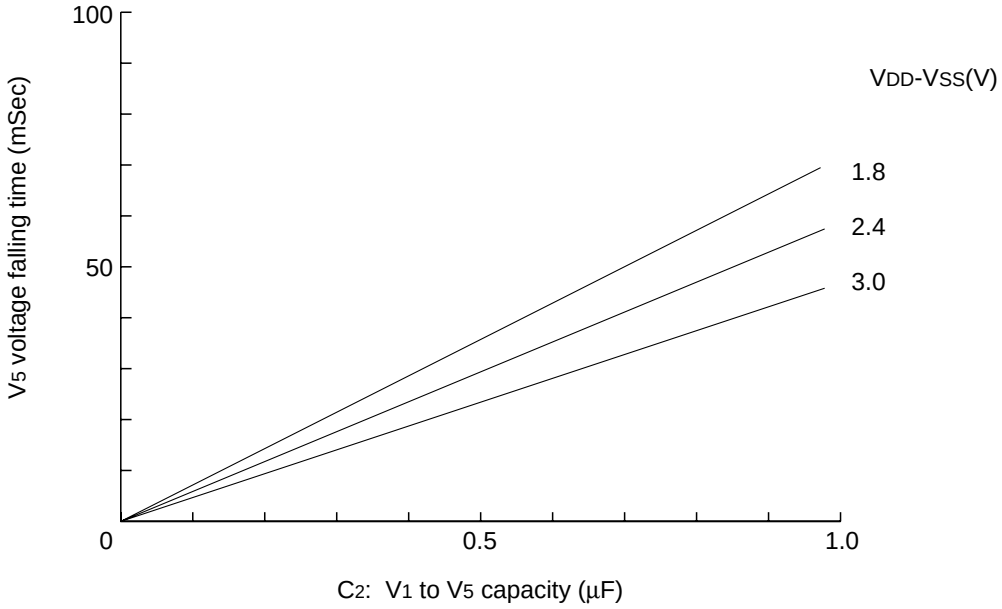


Figure 23

10. ABSOLUTE MAXIMUM RATINGS

Unless otherwise noted, V_{SS} = 0 V

Table 17

Parameter		Symbol	Conditions	Unit
Power Supply Voltage		V_{DD}	–0.3 to +6.0	V
Power supply voltage (2) (V_{DD} standard)		V_{SS2}	–4.0 to +0.3	V
Power supply voltage (3) (V_{DD} standard)		V_5, V_{OUT}	–18.0 to +0.3	V
Power supply voltage (4) (V_{DD} standard)		V_1, V_2, V_3, V_4	V_5 to +0.3	V
Input voltage		V_{IN}	–0.3 to V_{DD} + 0.3	V
Output voltage		V_O	–0.3 to V_{DD} + 0.3	V
Operating temperature		T_{OPR}	–40 to +85	°C
Storage temperature	TCP Bare chip	T_{STR}	–55 to +100 –55 to +125	°C

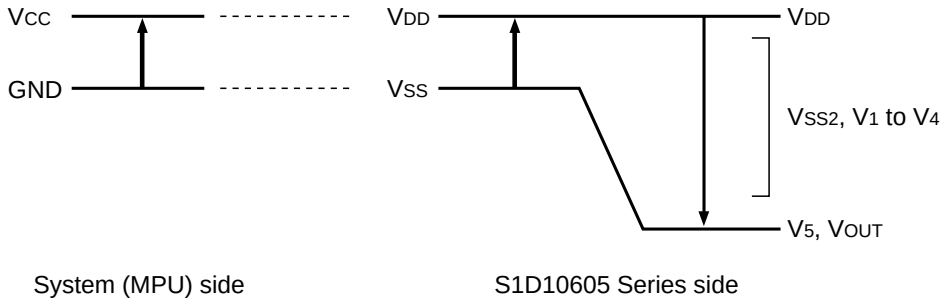


Figure 24

Notes and Cautions
1. The V_{SS2}, V_1 to V_5 and V_{OUT} are relative to the V_{DD} = 0V reference.
2. Insure that the voltage levels of V_1, V_2, V_3, and V_4 are always such that $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$.
3. Permanent damage to the LSI may result if the LSI is used outside of the absolute maximum ratings. Moreover, it is recommended that in normal operation the chip be used at the electrical characteristic conditions, and use of the LSI outside of these conditions may not only result in malfunctions of the LSI, but may have a negative impact on the LSI reliability as well.

11. DC CHARACTERISTICS

Unless otherwise specified, V_{SS} = 0 V, V_{DD} = 3.0 V ± 10%, Ta = –40 to 85°C

Table 18

Item		Symbol	Condition	Rating			Units	Applicable Pin
				Min.	Typ.	Max.		
Operating Voltage (1)	Recommended Voltage	V_{DD}		2.7	—	3.3	V	V_{DD}*1
	Possible Operating Voltage			1.8	—	3.6	V	V_{DD}*1
Operating Voltage (2)	Recommended Voltage	V_{SS2}	(Relative to V_{DD})	–3.3	—	–2.7	V	V_{SS2}
	Possible Operating Voltage	V_{SS2}	(Relative to V_{DD})	–4.0	—	–1.8	V	V_{SS2}
Operating Voltage (3)	Possible Operating Voltage	V_5	(Relative to V_{DD})	–14.0	—	–4.5	V	V_5 *2
	Possible Operating Voltage	V_1, V_2	(Relative to V_{DD})	0.4 × V_5	—	V_{DD}	V	V_1, V_2
	Possible Operating Voltage	V_3, V_4	(Relative to V_{DD})	V_5	—	0.6 × V_5	V	V_3, V_4
High-level Input Voltage		V_{IHC}		0.8 × V_{DD}	—	V_{DD}	V	*3
Low-level Input Voltage		V_{ILC}		V_{SS}	—	0.2 × V_{DD}	V	*3
High-level Output Voltage		V_{OHC}	I_{OH} = –0.5 mA	0.8 × V_{DD}	—	V_{DD}	V	*4
Low-level Output Voltage		V_{OLC}	I_{OL} = 0.5 mA	V_{SS}	—	0.2 × V_{DD}	V	*4
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS}	–1.0	—	1.0	µA	*5
Output leakage current		I_{LO}		–3.0	—	3.0	µA	*6
Liquid Crystal Driver ON Resistance		R_{ON}	Ta = 25°C (Relative To V_{DD}) V_5 = –14.0 V	—	2.0	3.5	kΩ	SEGn
			V_5 = –8.0 V	—	3.2	5.4	kΩ	COMn *7
Static Consumption Current		I_{SSQ}		—	0.01	5	µA	V_{SS}, V_{SS2}
Output Leakage Current		I_{5Q}	V_5 = –18.0 V (Relative To V_{DD})	—	0.01	15	µA	V_5
Input Terminal Capacitance		C_{IN}	Ta = 25°C f = 1 MHz	—	5	8	pF	
Oscillator Frequency	Internal Oscillator	f_{OSC}	Ta = 25°C	18	22	26	kHz	*8
	External Input	f_{CL}	S1D10605★★★★★/10607★★★★★	18	22	26	kHz	CL
	Internal Oscillator	f_{OSC}	Ta = 25°C	27	33	39	kHz	*8
	External Input	f_{CL}	S1D10606★★★★★/10608★★★★★/10609★★★★★	14	17	20	kHz	CL

Table 19

	Item	Symbol	Condition		Rating			Units	Applicable Pin
					Min.	Typ.	Max.		
Internal Power	Input voltage	V_{SS2}	With Quad (Relative To V_{DD})		–4.0	—	–1.8	V	V_{SS2}
	Supply Step-up output voltage Circuit	V_{OUT}	(Relative to V_{DD})		–16.0	—	—	V	V_{OUT}
	Voltage regulator Circuit Operating Voltage	V_{OUT}	(Relative to V_{DD})		–16.0	—	–6.0	V	V_{OUT}
	Voltage Follower Circuit Operating Voltage	V_5	(Relative to V_{DD})		–14.0	—	–4.5	V	V_5 *9
	Base Voltage	V_{REG0}	Ta = 25°C	–0.05%/°C	–2.04	–2.10	–2.16	V	*10

Note: 1. V_{DD}=0V is assumed for voltage V_{SS}, V_1 to V_5, and V_{OUT}.
2. Voltage V_1, V_2, V_3 and V_4 must always keep up the condition of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$.
3. If the LSI exceeds its absolute maximum rating, it may cause permanent damage. It is desirable to use it under electrical conditions during general operation. Otherwise, a malfunction of the LSI may be caused and may affect LSI reliability.
4. For the combined operating voltage of V_{DD} and V_5 systems, please refer to page 58, "Reference data 4, • Operating range of V_{DD} and V_5 systems."

- Dynamic Consumption Current (1), During Display, with the Internal Power Supply OFF
  Current consumed by total ICs when an external power supply is used.

Table 20 Display Pattern OFF

Ta = 25°C

Item	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
S1D10605*****	I_{DD} (1)	V_{DD} = 3.0 V, V_5 – V_{DD} = –11.0 V	—	16	27	µA	*11
S1D10606*****		V_{DD} = 3.0 V, V_5 – V_{DD} = –11.0 V	—	13	22		
		V_{DD} = 3.0 V, V_5 – V_{DD} = –8.0 V	—	9	15		
S1D10607*****		V_{DD} = 3.0 V, V_5 – V_{DD} = –8.0 V	—	7	12		
S1D10608*****/ S1D10609*****		V_{DD} = 3.0 V, V_5 – V_{DD} = –8.0 V	—	10	17		

Table 21 Display Pattern Checker

Ta = 25°C

Item	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
S1D10605*****	I_{DD} (1)	V_{DD} = 3.0 V, V_5 – V_{DD} = –11.0 V	—	21	35	µA	*11
S1D10606*****		V_{DD} = 3.0 V, V_5 – V_{DD} = –11.0 V	—	17	29		
		V_{DD} = 3.0 V, V_5 – V_{DD} = –8.0 V	—	12	20		
S1D10607*****		V_{DD} = 3.0 V, V_5 – V_{DD} = –8.0 V	—	10	17		
S1D10608*****/ S1D10609*****		V_{DD} = 3.0 V, V_5 – V_{DD} = –8.0 V	—	13	22		

- Dynamic Consumption Current (2), During Display, with the Internal Power Supply ON

Table 22 Display Pattern OFF

Ta = 25°C

Item	Symbol	Condition		Rating			Units	Notes
				Min.	Typ.	Max.		
S1D10605*****	I_{DD} (2)	V_{DD} = 3.0 V, Quad step-up voltage. V_5 – V_{DD} = –11.0 V	Normal Mode	—	100	150	µA	*12
			High-Power Mode	—	150	230		
S1D10606*****		V_{DD} = 3.0 V, Triple step-up voltage. V_5 – V_{DD} = –8.0 V	Normal Mode	—	59	99		
			High-Power Mode	—	95	159		
		V_{DD} = 3.0 V, Quad step-up voltage. V_5 – V_{DD} = –11.0 V	Normal Mode	—	91	152		
			High-Power Mode	—	139	232		
S1D10607*****		V_{DD} = 3.0 V, Triple step-up voltage. V_5 – V_{DD} = –8.0 V	Normal Mode	—	55	92		
			High-Power Mode	—	90	150		
S1D10608*****/ S1D10609*****		V_{DD} = 3.0 V, Triple step-up voltage. V_5 – V_{DD} = –8.0 V	Normal Mode	—	58	97		
			High-Power Mode	—	94	157		

Table 23 Display Pattern Checker

Ta = 25°C

Item	Symbol	Condition		Rating			Units	Notes
				Min.	Typ.	Max.		
S1D10605*****	I_{DD} (2)	V_{DD} = 3.0 V, Quad step-up voltage. $V_5 - V_{DD}$ = –11.0 V	Normal Mode	—	120	180	µA	*12
			High-Power Mode	—	170	255		
S1D10606*****		V_{DD} = 3.0 V, Triple step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	67	112		
			High-Power Mode	—	103	172		
		V_{DD} = 3.0 V, Quad step-up voltage. $V_5 - V_{DD}$ = –11.0 V	Normal Mode	—	105	175		
			High-Power Mode	—	158	225		
S1D10607*****		V_{DD} = 3.0 V, Triple step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	60	100		
			High-Power Mode	—	98	164		
S1D10608*****/ S1D10609*****		V_{DD} = 3.0 V, Triple step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	67	112		
			High-Power Mode	—	104	174		

- Consumption Current at Time of Power Saver Mode, V_{SS} = 0 V, V_{DD} = 3.0 V ± 10%

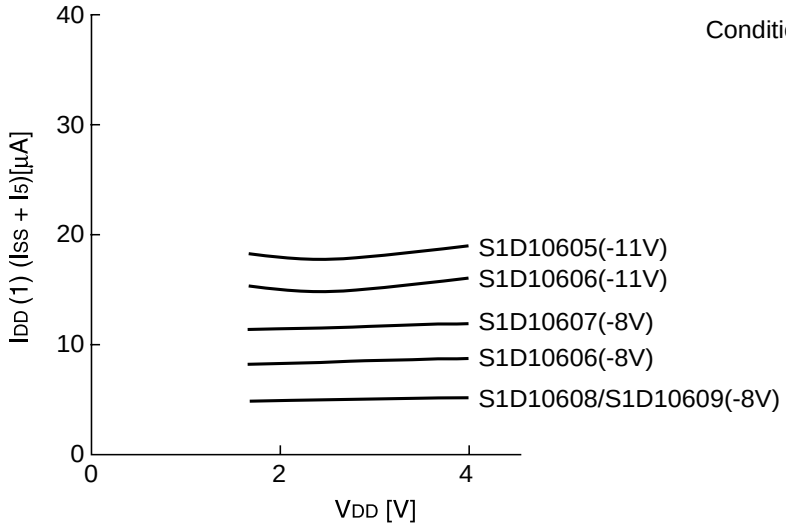
Table 24

Ta = 25°C

Item	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Sleep mode S1D10605*****	I_{DDS1}	—	—	0.01	5	µA	
Standby Mode S1D10605*****	I_{DDS2}	—	—	4	8		
Sleep mode S1D10606*****	I_{DDS1}	—	—	0.01	5		
Standby Mode S1D10606*****	I_{DDS2}	—	—	4	8		
Sleep mode S1D10607*****	I_{DDS1}	—	—	0.01	5		
Standby Mode S1D10607*****	I_{DDS2}	—	—	3	6		
Sleep mode S1D10608*****/ S1D10609*****	I_{DDS1}	—	—	0.01	5		
Standby Mode S1D10608*****/ S1D10609*****	I_{DDS2}	—	—	4	8		

Reference Data 1

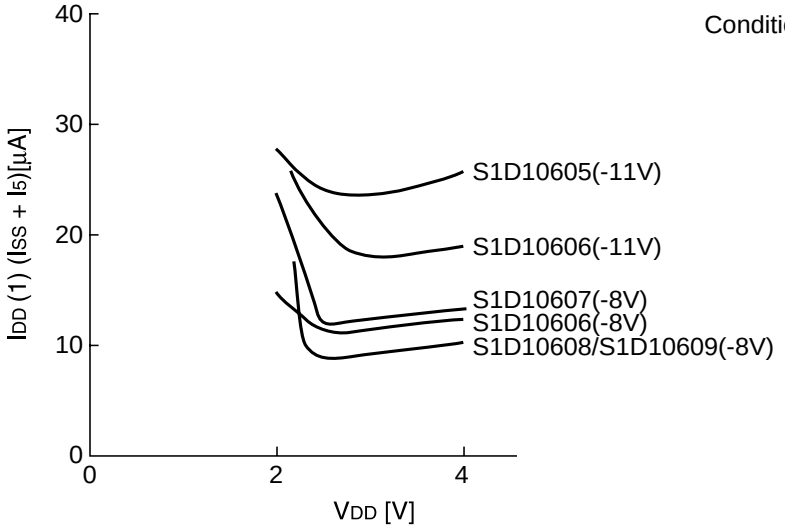
- Dynamic Consumption Current (1) During LCD Display Using an External Power Supply



Conditions: Internal power supply OFF
External power supply in use
S1D10605/S1D10606 (–11.0V):
$V_5 – V_{DD}$ = –11.0 V
S1D10606 (–8.0V)/S1D10607/
S1D10608/S1D10609:
$V_5 – V_{DD}$ = –8.0 V
Display pattern: OFF
Ta = 25°C

Note: *11

Figure 25



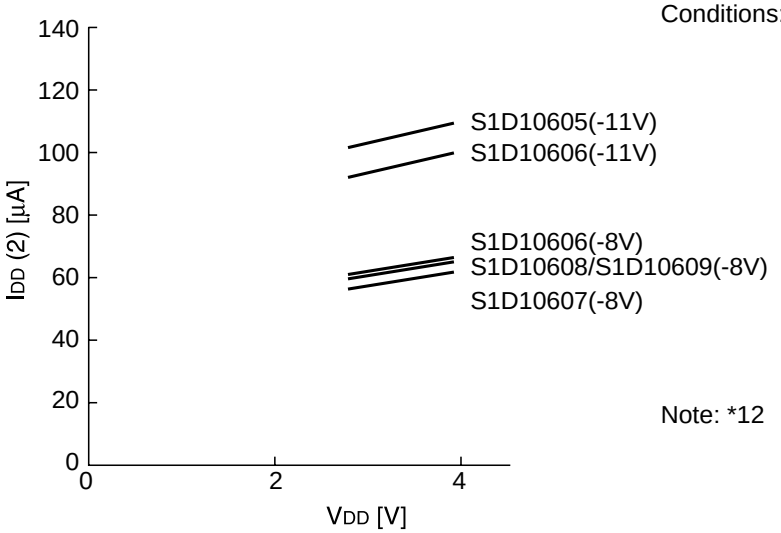
Conditions: Internal power supply OFF
External power supply in use
S1D10605/S1D10606 (–11.0V):
$V_5 – V_{DD}$ = –11.0 V
S1D10606 (–8.0V)/S1D10607/
S1D10608/S1D10609:
$V_5 – V_{DD}$ = –8.0 V
Display pattern: Checker
Ta = 25°C

Note: *11

Figure 26

Reference Data 2

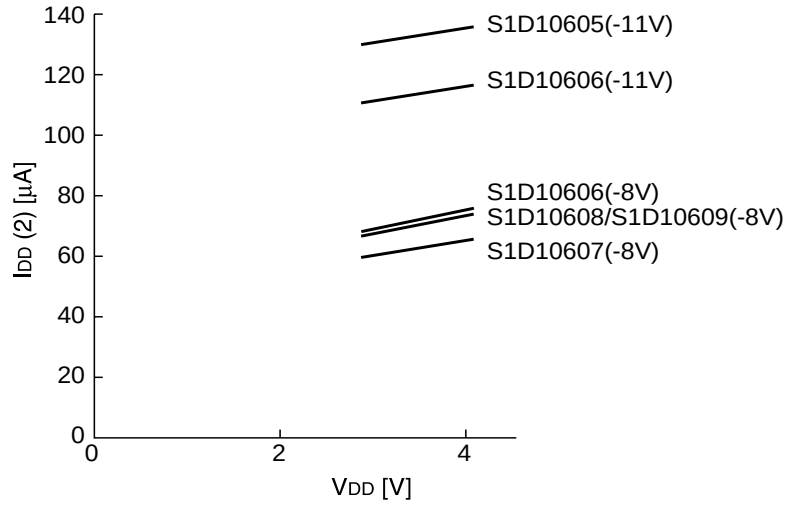
- Dynamic Consumption Current (2) During LCD display using the internal power supply



Conditions: Internal power supply ON
S1D10605/S1D10606 (×4, –11.0V):
4× step-up voltage: $V_5 – V_{DD}$ = –11.0 V
S1D10606 (×3, –8.0V)/S1D10607/
S1D10608/S1D10609:
3× step-up voltage: $V_5 – V_{DD}$ = –8.0 V
Normal mode
Display pattern: OFF
Ta = 25°C

Note: *12

Figure 27



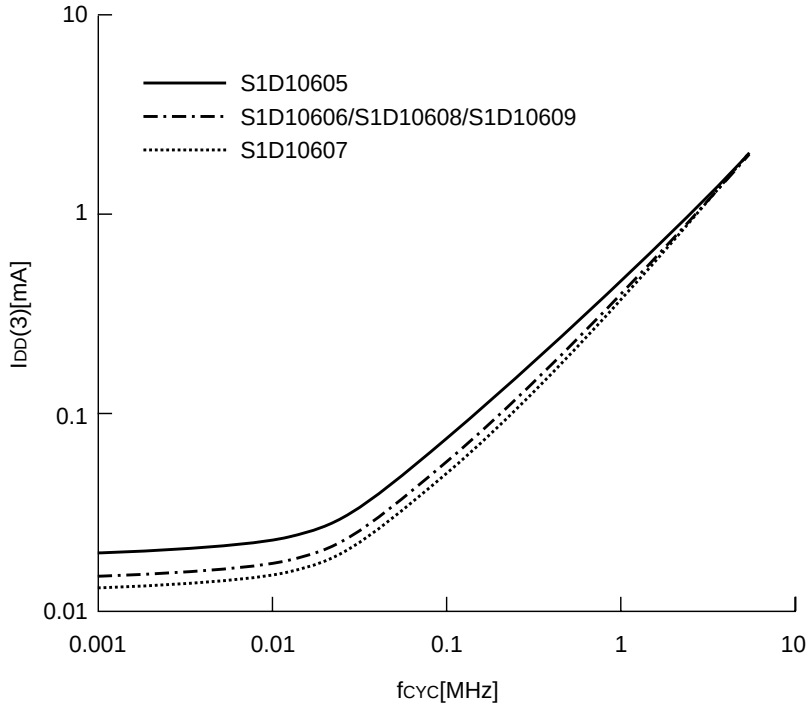
Conditions: Internal power supply ON
S1D10605/S1D10606 (×4, –11.0V):
4× step-up voltage: $V_5 – V_{DD}$ = –11.0 V
S1D10606 (×3, –8.0V)/S1D10607/
S1D10608/S1D10609:
3× step-up voltage: $V_5 – V_{DD}$ = –8.0 V
Normal mode
Display pattern: Checker
Ta = 25°C

Note: *12

Figure 28

Reference Data 3

- Dynamic Consumption Current (3) During access



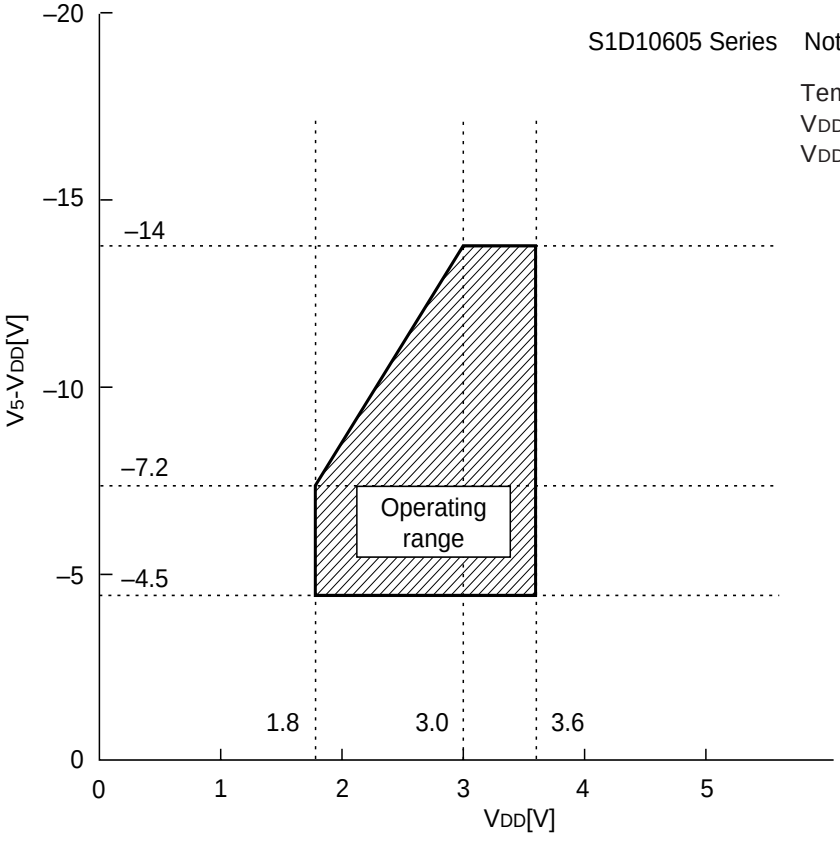
This figure indicates the consumption current while the checker pattern is constantly written through f_{CYC}.
If there is no access, then only (1) remains.

Conditions: Internal power supply OFF, external power supply used
S1D10605:
$V_{DD} - V_{SS}$ = 3.0 V, V_5=–11.0 V
S1D10606/S1D10607/S1D10608/S1D10609:
$V_{DD} - V_{SS}$ = 3.0 V, V_5=–8.0 V
Ta = 25°C

Figure 29

Reference Data 4

- Operating voltage range of V_{SS} and V_5 systems



S1D10605 Series Note: *2

Temperature condition :
$V_{DD} - V_{SS}$ = 1.8 to 2.2V : Ta = –10 to 85°C
$V_{DD} - V_{SS}$ = 2.2 to 3.6V : Ta = –40 to 85°C

Figure 30

- The Relationship Between Oscillator Frequency f_{OSC}, Display Clock Frequency f_{CL} and the Liquid Crystal Frame Rate Frequency f_{FR}

Table 25

Item		f_{CL}	f_{FR}
S1D10605*****	When the internal oscillator circuit is used	$\frac{f_{OSC}}{4}$	$\frac{f_{OSC}}{4 \times 65}$
	When the internal oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{260}$
S1D10606*****	When the internal oscillator circuit is used	$\frac{f_{OSC}}{8}$	$\frac{f_{OSC}}{8 \times 49}$
	When the internal oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{196}$
S1D10607*****	When the internal oscillator circuit is used	$\frac{f_{OSC}}{8}$	$\frac{f_{OSC}}{8 \times 33}$
	When the internal oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{264}$
S1D10608*****	When the internal oscillator circuit is used	$\frac{f_{OSC}}{8}$	$\frac{f_{OSC}}{8 \times 55}$
	When the internal oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{220}$
S1D10609*****	When the internal oscillator circuit is used	$\frac{f_{OSC}}{8}$	$\frac{f_{OSC}}{8 \times 53}$
	When the internal oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{212}$

(f_{FR} is the liquid crystal alternating current period, and not the FR signal period.)

References for items market with *

*1 While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.

*2 The operating voltage range for the V_{DD} system and the V_5 system is as shown in Figure 30. This applies when the external power supply is being used.

*3 The A0, D0 to D5, D6 (SCL), D7 (SI), $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CLS, CL, FR, M/S, C86, P/S, $\overline{DOF}$, $\overline{RES}$, IRS, and $\overline{HPM}$ terminals.

*4 The D0 to D7, FR, FRS, $\overline{DOF}$, and CL terminals.

*5 The A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CLS, M/S, C86, P/S, $\overline{RES}$, IRS, and $\overline{HPM}$ terminals.

*6 Applies when the D0 to D5, D6 (SCL), D7 (SI), CL, FR, and $\overline{DOF}$ terminals are in a high impedance state.

*7 These are the resistance values for when a 0.1 V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V_1, V_2, V_3, and V_4). These are specified for the operating voltage (3) range.
R_{ON} = 0.1 V/Δ I (Where Δ I is the current that flows when 0.1 V is applied while the power supply is ON.)

*8 See Table 9-7 for the relationship between the oscillator frequency and the frame rate frequency.

*9 The V_5 voltage regulator circuit regulates within the operating voltage range of the voltage follower.

*10 This is the internal voltage reference supply for the V_5 voltage regulator circuit. In the S1D10605 Series chips, the temperature range can come in three types as V_{REG} options: (1) approximately –0.05%/°C, (2) –0.2%/°C, and (3) external input.

*11, 12 It indicates the current consumed on ICs alone when the internal oscillator circuit and display are turned on.
The S1D10605 is 1/9 biased, S1D10606/S1D10608/S1D10609 is 1/8 biased and S1D10607 is 1/6 biased.
Does not include the current due to the LCD panel capacity and wiring capacity.
Applicable only when there is no access from the MPU.

*12 It is the value on a model having the V_{REG} option temperature gradient is –0.05%/°C when the V_5 voltage regulator internal resistor is used.

Timing Characteristics

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

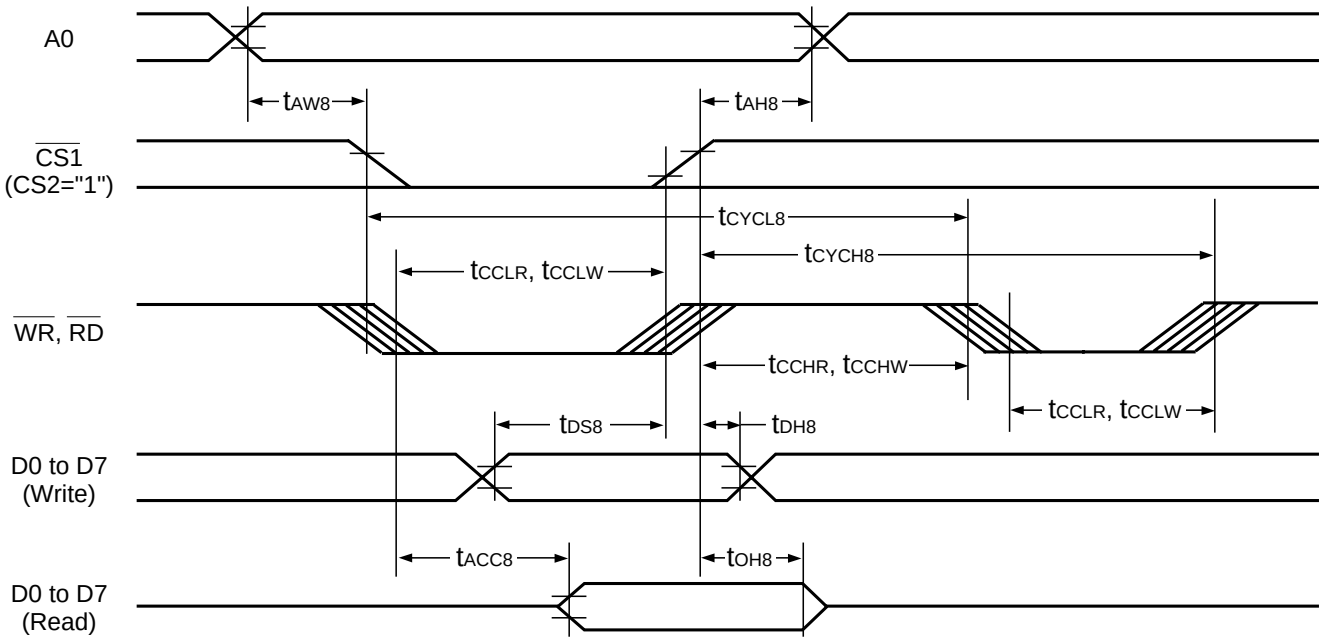


Figure 31

Table 26

(V_{DD} = 2.7 V to 3.6 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	ns
System cycle time 1	A0	t_{CYCL8}		300	—	ns
System cycle time 2		t_{CYCH8}		300	—	ns
Control LOW pulse width (Write)	$\overline{WR}$	t_{CCLW}		60	—	ns
Control LOW pulse width (Read)	$\overline{RD}$	t_{CCLR}		120	—	ns
Control HIGH pulse width (Write)	$\overline{WR}$	t_{CCHW}		60	—	ns
Control HIGH pulse width (Read)	$\overline{RD}$	t_{CCHR}		60	—	ns
Data setup time	D0 to D7	t_{DS8}		40	—	ns
Data hold time		t_{DH8}		15	—	ns
$\overline{RD}$ access time		t_{ACC8}	CL = 100 pF	—	140	ns
Output disable time		t_{OH8}		10	100	ns

Table 27

(V_{DD} = 2.4 V to 3.0 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	ns
System cycle time 1	A0	t_{CYCL8}		450	—	ns
System cycle time 2		t_{CYCH8}		450	—	ns
Control LOW pulse width (Write)	$\overline{WR}$	t_{CCLW}		90	—	ns
Control LOW pulse width (Read)	$\overline{RD}$	t_{CCLR}		180	—	ns
Control HIGH pulse width (Write)	$\overline{WR}$	t_{CCHW}		90	—	ns
Control HIGH pulse width (Read)	$\overline{RD}$	t_{CCHR}		90	—	ns
Data setup time	D0 to D7	t_{DS8}		60	—	ns
Data hold time		t_{DH8}		20	—	ns
$\overline{RD}$ access time		t_{ACC8}	CL = 100 pF	—	230	ns
Output disable time		t_{OH8}		10	150	ns

Table 28

(V_{DD} = 1.8 V to 2.4 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	ns
System cycle time 1	A0	t_{CYCL8}		600	—	ns
System cycle time 2		t_{CYCH8}		600	—	ns
Control LOW pulse width (Write)	$\overline{WR}$	t_{CCLW}		120	—	ns
Control LOW pulse width (Read)	$\overline{RD}$	t_{CCLR}		240	—	ns
Control HIGH pulse width (Write)	$\overline{WR}$	t_{CCHW}		120	—	ns
Control HIGH pulse width (Read)	$\overline{RD}$	t_{CCHR}		120	—	ns
Data setup time	D0 to D7	t_{DS8}		80	—	ns
Data hold time		t_{DH8}		30	—	ns
$\overline{RD}$ access time		t_{ACC8}	CL = 100 pF	—	280	ns
Output disable time		t_{OH8}		10	200	ns

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, $(t_r + t_f) \leq (t_{CYCL\,(H)\,8} - t_{CCLW} - t_{CCHW})$ for $(t_r + t_f) \leq (t_{CYCL\,(H)\,8} - t_{CCLR} - t_{CCHR})$ are specified.

*2 All timing is specified using 20% and 80% of V_{DD} as the reference.

*3 t_{CCLW} and t_{CCLR} are specified as the overlap between CS1 being LOW (CS2 = HIGH) and $\overline{WR}$ and $\overline{RD}$ being at the LOW level.

System Bus Read/Write Characteristics 2 (6800 Series MPU)

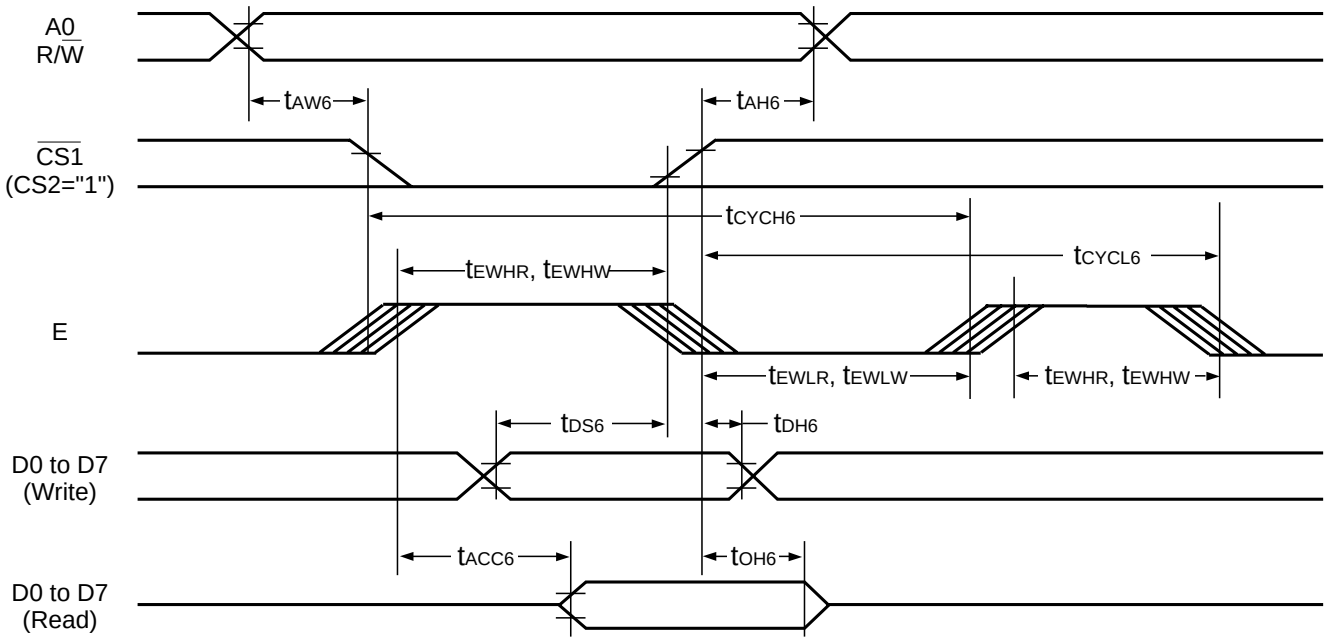


Figure 32

Table 29

(V_{DD} = 2.7 V to 3.6 V, Ta = –40 to 85°C)

Item		Signal	Symbol	Condition	Rating		Units
					Min.	Max.	
Address hold time Address setup time		A0	t_{AH6} t_{AW6}		0 0	— —	ns ns
System cycle time 1 System cycle time 2		A0	t_{CYCH6} t_{CYCL6}		300 300	— —	ns ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		40 15	— —	ns ns
Access time Output disable time			t_{ACC6} t_{OH6}	CL = 100 pF	— 10	140 100	ns ns
Enable HIGH pulse time	Read Write	E	t_{EWHR} t_{EWHW}		120 60	— —	ns ns
Enable LOW pulse time	Read Write	E	t_{EWLR} t_{EWLW}		60 60	— —	ns ns

Table 30

(V_{DD} = 2.4 V to 3.0 V, Ta = –40 to 85°C)

Item		Signal	Symbol	Condition	Rating		Units
					Min.	Max.	
Address hold time Address setup time		A0	t_{AH6} t_{AW6}		0 0	— —	ns ns
System cycle time 1 System cycle time 2		A0	t_{CYCH6} t_{CYCL6}		450 450	— —	ns ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		60 20	— —	ns ns
Access time Output disable time			t_{ACC6} t_{OH6}	CL = 100 pF	— 10	230 150	ns ns
Enable HIGH pulse time	Read Write	E	t_{EWHR} t_{EWHW}		180 90	— —	ns ns
Enable LOW pulse time	Read Write	E	t_{EWLR} t_{EWLW}		90 90	— —	ns ns

Table 31

(V_{DD} = 1.8 V to 2.4 V, Ta = –40 to 85°C)

Item		Signal	Symbol	Condition	Rating		Units
					Min.	Max.	
Address hold time Address setup time		A0	t_{AH6} t_{AW6}		0 0	— —	ns ns
System cycle time 1 System cycle time 2		A0	t_{CYCH6} t_{CYCL6}		600 600	— —	ns ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		80 30	— —	ns ns
Access time Output disable time			t_{ACC6} t_{OH6}	CL = 100 pF	— 10	280 200	ns ns
Enable HIGH pulse time	Read Write	E	t_{EWHR} t_{EWHW}		240 120	— —	ns ns
Enable LOW pulse time	Read Write	E	t_{EWLR} t_{EWLW}		120 120	— —	ns ns

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, $(t_r + t_f) \leq (t_{CYCH\,(L)\,6} - t_{EWLW} - t_{EWHW})$ for $(t_r + t_f) \leq (t_{CYCH\,(L)\,6} - t_{EWLR} - t_{EWHR})$ are specified.
*2 All timing is specified using 20% and 80% of V_{DD} as the reference.
*3 t_{EWLW} and t_{EWLR} are specified as the overlap between $\overline{CS1}$ being LOW (CS2 = HIGH) and E.

The Serial Interface

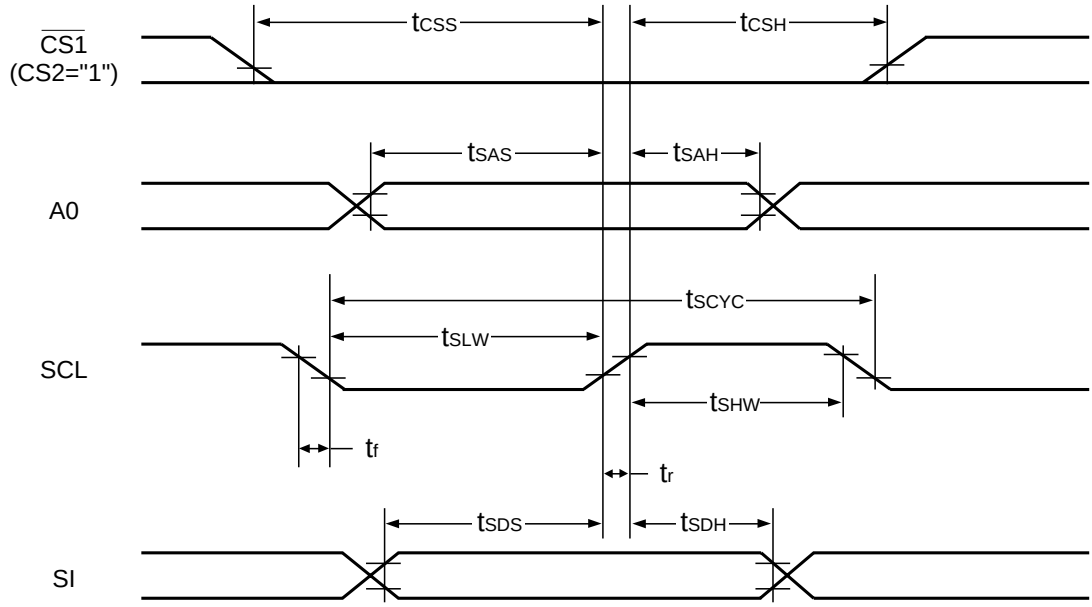


Figure 33

Table 32

(V_{DD} = 2.7 V to 3.6 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		250	—	ns
SCL HIGH pulse width		t_{SHW}		100	—	ns
SCL LOW pulse width		t_{SLW}		100	—	ns
Address setup time	A0	t_{SAS}		150	—	ns
Address hold time		t_{SAH}		150	—	ns
Data setup time	SI	t_{SDS}		100	—	ns
Data hold time		t_{SDH}		100	—	ns
CS-SCL time	CS	t_{CSS}		150	—	ns
		t_{CSH}		150	—	ns

Table 33

(V_{DD} = 2.4 V to 3.0 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		300	—	ns
SCL HIGH pulse width		t_{SHW}		125	—	ns
SCL LOW pulse width		t_{SLW}		125	—	ns
Address setup time	A0	t_{SAS}		200	—	ns
Address hold time		t_{SAH}		200	—	ns
Data setup time	SI	t_{SDS}		125	—	ns
Data hold time		t_{SDH}		125	—	ns
CS-SCL time	CS	t_{CSS}		200	—	ns
		t_{CSH}		200	—	ns

Table 34

(V_{DD} = 1.8 V to 2.4 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		400	—	ns
SCL HIGH pulse width		t_{SHW}		150	—	ns
SCL LOW pulse width		t_{SLW}		150	—	ns
Address setup time	A0	t_{SAS}		250	—	ns
Address hold time		t_{SAH}		250	—	ns
Data setup time	SI	t_{SDS}		150	—	ns
Data hold time		t_{SDH}		150	—	ns
CS-SCL time	CS	t_{CSS}		250	—	ns
		t_{CSH}		250	—	ns

*1 The input signal rise and fall time (t_r, t_f) are specified at 15 ns or less.
*2 All timing is specified using 20% and 80% of V_{DD} as the standard.

Display Control Output Timing

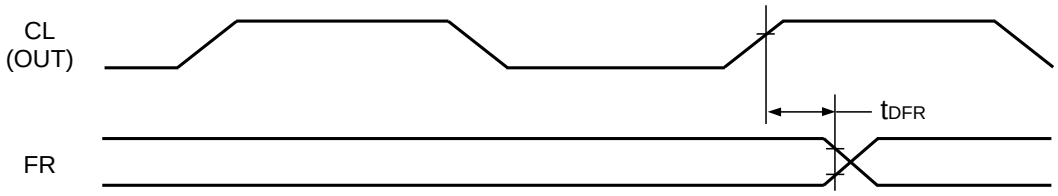


Figure 34

Table 35

(V_{DD} = 2.7 V to 3.6 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	CL = 50 pF	—	15	60	ns

Table 36

(V_{DD} = 2.4 V to 3.0 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	CL = 50 pF	—	20	80	ns

Table 37

(V_{DD} = 1.8 V to 2.4 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	CL = 50 pF	—	30	120	ns

*1 Valid only when the master mode is selected.
*2 All timing is based on 20% and 80% of V_{DD}.

Reset Timing

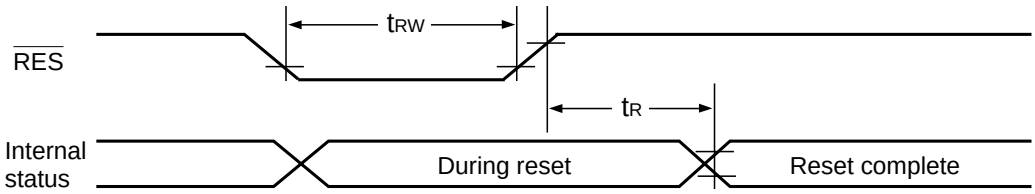


Figure 35

Table 38

(V_{DD} = 2.7 V to 3.6 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		—	—	1	µs
Reset LOW pulse width	RES	t_{RW}		1	—	—	µs

Table 39

(V_{DD} = 2.4 V to 3.0 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		—	—	1.3	µs
Reset LOW pulse width	RES	t_{RW}		1.3	—	—	µs

Table 40

(V_{DD} = 1.8 V to 2.4 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		—	—	1.5	µs
Reset LOW pulse width	RES	t_{RW}		1.5	—	—	µs

*1 All timing is specified with 20% and 80% of V_{DD} as the standard.

12. THE MPU INTERFACE (REFERENCE EXAMPLES)

The S1D10605 Series can be connected to either 80 × 86 Series MPUs or to 6800 Series MPUs. Moreover, using the serial interface it is possible to operate the S1D10605 series chips with fewer signal lines.
The display area can be enlarged by using multiple S1D10605 Series chips. When this is done, the chip select signal can be used to select the individual ICs to access.

(1) 8080 Series MPUs

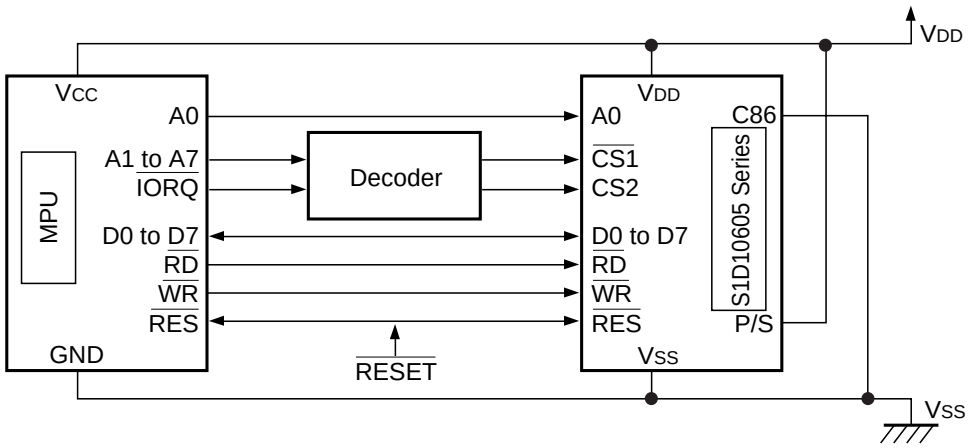


Figure 36

(2) 6800 Series MPUs

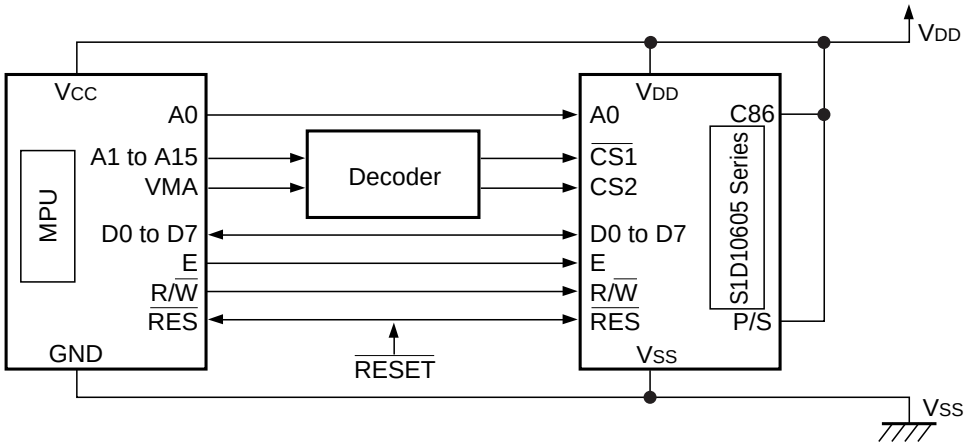


Figure 37

(3) Using the Serial Interface

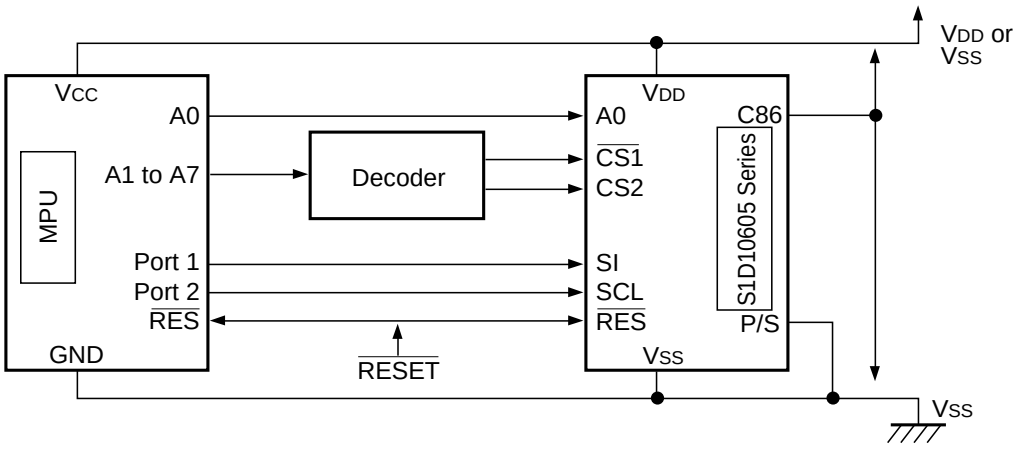


Figure 38

13. CONNECTIONS BETWEEN LCD DRIVERS (REFERENCE EXAMPLE)

The liquid crystal display area can be enlarged with ease through the use of multiple S1D10605 Series chips. Use a same equipment type.

(1) S1D10605 (master) ↔ S1D10605 (slave)

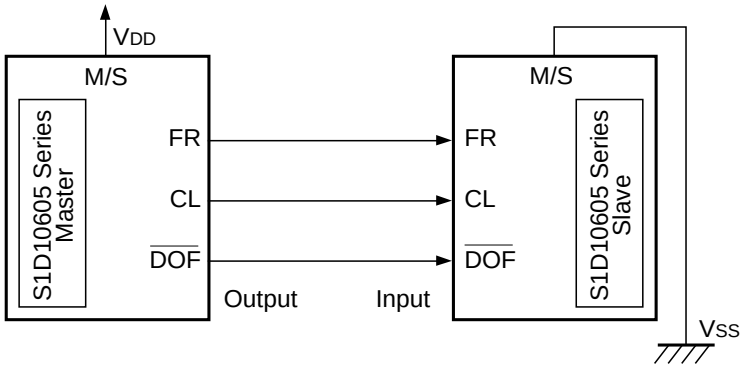


Figure 39

14. CONNECTIONS BETWEEN LCD DRIVERS (REFERENCE EXAMPLES)

The liquid crystal display area can be enlarged with ease through the use of multiple S1D10605 Series chips. Use a same equipment type, in the composition of these chips.

(1) Single-chip Structure

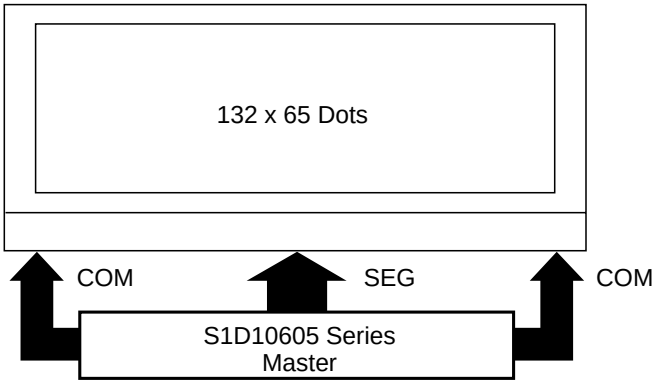


Figure 40

(2) Double-chip Structure, #1

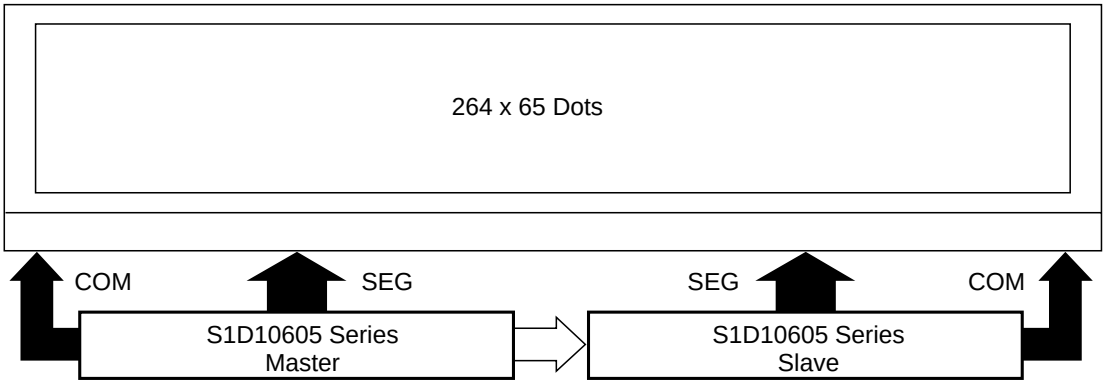


Figure 41

15. CAUTIONS

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"Cautions pertaining to light"
Semiconductor devices are highly sensitive to light, causing changes in their properties. Malfunctions may occur when light is applied to the IC. To avoid such malfunctions, please consider the following when installing to circuit boards or any other products.
(1) Make sure the IC is installed in a light-resistant structure.
(2) IC should be inspected under a light-resistant environment.
(3) Make sure no light will be applied to all four surfaces of the IC chip.