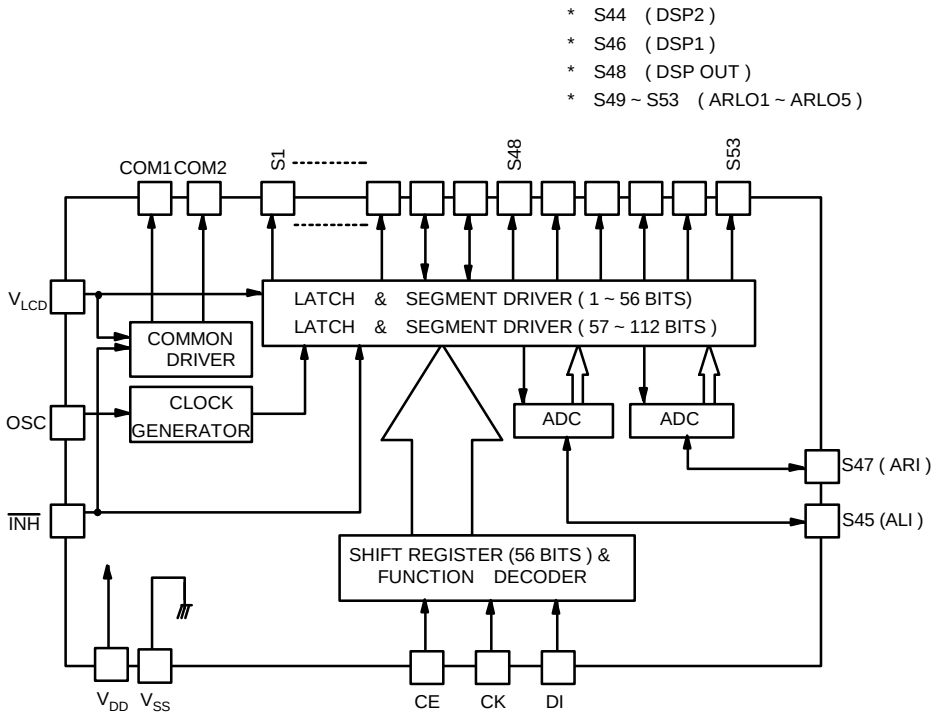
INTRODUCTION

The KS0035 is a general purpose LCD driving IC,
and designed to be available for electronic frequency tuning
display applications or microcomputer application systems.

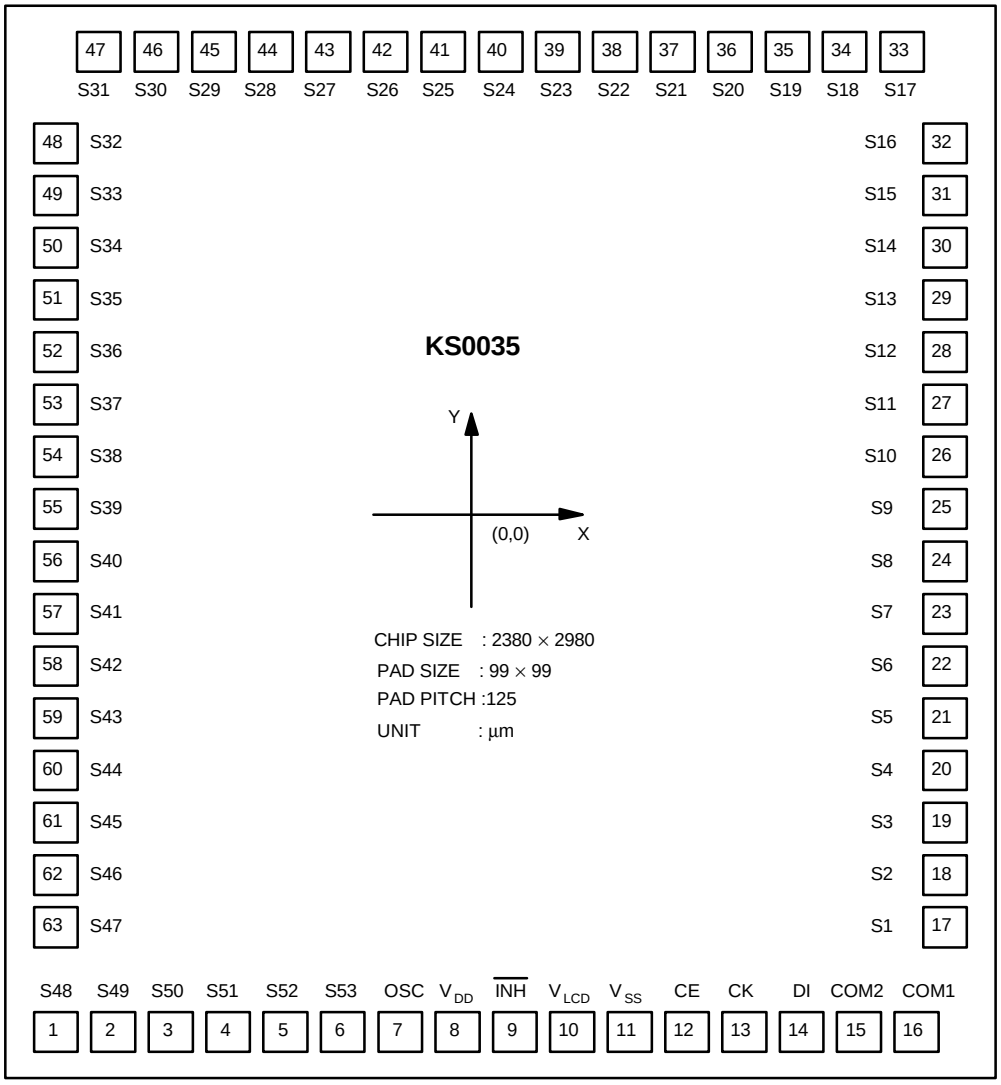
FEATURES

. Maximum 53 segment output for static display.
. Drive system : 1/1 duty → 53 segments
1/2 duty → 104 segments.
. 3 input pins for serial data transfer (CE , CK , DI)
. 2 pins for 5 - level - AD converter (ARI , ALI)
. 2 display pins for direct displaying (DSP1 , DSP2)
. $\overline{INH}$ pin for blinking out display.

BLOCK DIAGRAM



PAD DIAGRAM



* There is mark of KS0035 on the center in chip.

PAD LOCATION

UNIT(μm)

PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE	
		X	Y			X	Y
1	S48	-960	-1265	33	S17	885	1265
2	S49	-835	-1265	34	S18	760	1265
3	S50	-710	-1265	35	S19	635	1265
4	S51	-585	-1265	36	S20	510	1265
5	S52	-460	-1265	37	S21	385	1265
6	S53	-335	-1265	38	S22	260	1265
7	OSC	-140	-1265	39	S23	135	1265
8	V_{DD}	-15	-1265	40	S24	10	1265
9	/INH	110	-1265	41	S25	-115	1265
10	V_{LCD}	235	-1265	42	S26	-240	1265
11	V_{SS}	360	-1265	43	S27	-365	1265
12	CE	485	-1265	44	S28	-490	1265
13	CK	610	-1265	45	S29	-615	1265
14	DI	735	-1265	46	S30	-740	1265
15	COM2	860	-1265	47	S31	-865	1265
16	COM1	985	-1265	48	S32	-965	940
17	S1	965	-970	49	S33	-965	815
18	S2	965	-845	50	S34	-965	690
19	S3	965	-720	51	S35	-965	565
20	S4	965	-595	52	S36	-965	440
21	S5	965	-470	53	S37	-965	315
22	S6	965	-345	54	S38	-965	190
23	S7	965	-220	55	S39	-965	65
24	S8	965	-95	56	S40	-965	-60
25	S9	965	30	57	S41	-965	-185
26	S10	965	155	58	S42	-965	-310
27	S11	965	280	59	S43	-965	-435
28	S12	965	405	60	S44	-965	-560
29	S13	965	530	61	S45	-965	-685
30	S14	965	655	62	S46	-965	-810
31	S15	965	780	63	S47	-965	-935
32	S16	965	905				

PAD DESCRIPTION

PAD	INPUT/OUTPUT	NAME	DESCRIPTION	INTERFACE
V_{DD}	Power	Operating Voltage	For logic circuit (2.7V~6.5V)	Power Supply
V_{SS}			0V (GND)	
V_{LCD}		Driver Supply Voltage	Power supply for driving LCD	
COM1, COM2	Output	Common output	- 1/1duty: Only COM1 is used, COM2 open - 1/2duty: Both COM1 and COM2 are used.	LCD
S1~S43	Output	Segment output	Segment output for driving LCD	LCD
S46(DSP1) S44(DSP2)	Output Input	Segment output DSP input	Segment output for driving LCD (Display input pins)	LCD Display input
S47(ARI) S45(ALI)	Output Input	Segment output Analog input	Segment output for driving LCD (Analog input pins)	LCD Analog input
S48 (DSPOUT)	Output	Segment output DSP output	Segment output for driving LCD (DSP output pins)	LCD
S49~S53 (ARLO1~5)	Output	Segment output Analog output	Segment output for driving LCD (Analog output pins)	LCD
OSC	Input	Oscillator	Input for clock generator	Resistor, Capacitor
CE	Input	Chip Enable	CE = High P Chip Enable status	Controller
CK	Input	Data Shift Clock	Clock pulse input for the 1bit serial shift register. The data is shifted to 56 bit shift register at the rising edge of the clock.	Controller
DI	Input	Data Input	Display data input	Controller
$\overline{INH}$	Input	Display blinking	Display blinking input ($\overline{INH}$ = LOW)	Controller

MAXIMUM ABSOLUTE LIMIT(Ta=25°C, VSS=0V)

Characteristic	Symbol	Value	Applicable pin	Unit
Maximum Supply Voltage	V_{DDmax}	-0.3 ~ +7.0	V_{DD}	V
	$V_{LCD\ max}$	-0.3 ~ V_{DD}+0.3	V_{LCD}	V
Input Voltage	V_{IN1}	-0.3 ~ V_{DD}+0.3	CE, CK, DI, $\overline{INH}$	V
	V_{IN2}	-0.3 ~ V_{DD}+0.3	S44 ~ S47 Output off(Used as ARI, ALI DSP1, DSP2)	V
	V_{IN3}	-0.3 ~ V_{DD}+0.3	OSC, output off	V
Output Voltage	V_O	-0.3 ~ V_{DD}+0.3	OSC, output off	V
Output Current	I_{O1}	100	S1 ~ S53	μA
	I_{O2}	1.0	COM1, COM2	mA
Allowable Power Dissipation	P_{Dmax}	100	Ta=85°C	mW
Operating Temperature	T_{OPR}	-30 ~ +85	-	°C
Storage Temperature	T_{STG}	-40 ~ +125	-	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics (V_{DD}=2.7V ~ 6,5V, V_{SS}=0V, V_{LCD}=2.7V ~ V_{DD}, T_a= - 30 ~ + 85 °C)

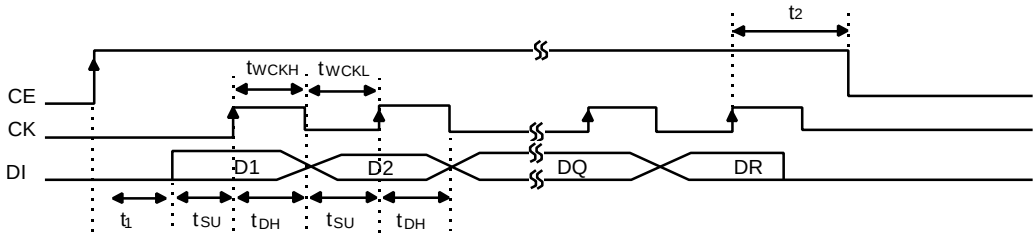
Characteristics	Symbol	Test Conditions		Min	Typ	Max	Unit
Operating Voltage	V_{DD}	-		2.7	-	6.5	V
Driver Supply Voltage	V_{LCD}	-		2.7	-	V_{DD}	
Input ¡HIGH¡± Vdt age	V_{IH1}	CE, CK, DI, $\overline{INH}$		$0.8V_{DD}$	-	V_{DD}	
Input ¡LOW¡ Voltage 1	V_{IL1}			0	-	$0.2V_{DD}$	
Input ¡HIGH¡ Voltage 2	V_{IH2}	S44, S46		$0.8V_{DD}$	-	V_{DD}	
Input ¡LOW¡ Voltage 2	V_{IL2}	Output off(Used input pin DSP1, DSP2)		0	-	$0.2V_{DD}$	
Input ¡HIGH¡ Current 1	I_{IH1}	CE, CK, DI, $\overline{INH}$(V_I=V_{DD})		-	-	5.0	µA
Input ¡LOW¡ Current 1	I_{IL1}	CE, CK, DI, $\overline{INH}$(V_I=0V)		-	-	5.0	
Input ¡HIGH¡ Current 2	I_{IH2}	S44, S45, S46, S47(V_I=V_{DD})		-	-	10.0	
Input ¡LOW¡ Current 2	I_{IL2}	S44, S45, S46, S47(V_I=0V)		-	-	10.0	
Output ¡HIGH¡ Voltage 1	V_{OH1}	S1 ~ S53(V_{LCD}=3V, I_O=-10µA)		V_{LCD}-0.5	-	-	V
Output ¡LOW¡ Voltage 1	V_{OL1}	S1 ~ S53(V_{LCD}=3V, I_O=+10 µA)		-	-	0.5	
Output ¡HIGH¡ Voltage 2	V_{OH2}	COM1, COM2(V_{LCD}=3V, I_O=-100 µA)		V_{LCD}-0.6	-	-	
Output ¡LOW¡ Voltage 2	V_{OL2}	COM1, COM2(V_{LCD}=3V, I_O = +100 µA)		-	-	0.6	
Medium Voltage	V_{M1}	COM1, COM2(V_{LCD}=6.5V, I_O=±100 µA)		2.65	3.25	3.85	
	V_{M2}	COM1, COM2(V_{LCD}=3.0V, I_O=±100 µA)		0.9	1.5	2.1	
First Step Lighting Voltage	V_{A1}	S45, S47		$0.07V_{DD}$	$0.1V_{DD}$	$0.13V_{DD}$	
Second Step Lighting Voltage	V_{A2}	S45, S47		$0.17V_{DD}$	$0.2V_{DD}$	$0.23V_{DD}$	
Third Step Lighting Voltage	V_{A3}	S45, S47		$0.27V_{DD}$	$0.3V_{DD}$	$0.33V_{DD}$	
Fourth Step Lighting Voltage	V_{A4}	S45, S47		$0.37V_{DD}$	$0.4V_{DD}$	$0.43V_{DD}$	
Fifth Step Lighting Voltage	V_{A5}	S45, S47		$0.47V_{DD}$	$0.5V_{DD}$	$0.53V_{DD}$	
Step Voltage Difference	V_{STEP}	S45, S47 (refer to Fig. 2)		$0.09V_{DD}$	$0.1V_{DD}$	$0.11V_{DD}$	
Oscillation Frequency	f_{OSC}	OSC(R=51KΩ, C=680pF)		40	50	60	KHz
Operating Current	I_{DD1}	V_{DD}=3V	f_{CK}=2MHz	-	0.2	0.4	mA
	I_{DD2}	V_{DD}=6.5V	R=51KΩ	-	0.4	0.8	
Driving Current	I_{LCD1}	V_{LCD}=3V	C=680pF	-	0.6	1	
	I_{LCD2}	V_{LCD}=6.5V		-	1.2	2	

AC CHARACTERISTICS (V_{SS}=0V, V_{DD}=2.7V~ 6.5V, V_{LCD}=2.7V ~ V_{DD}, Ta= - 30 ~ + 85 °C)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Pulse Width		t_{WCKH}	V_{DD}=5.0V	0.25	-	-	µs
		t_{WCKL}	V_{DD}=5.0V	0.25	-	-	
Data Set-up Time		t_{SU}	V_{DD}=5.0V	0.25	-	-	
Data Hold Time		t_{DH}	V_{DD}=5.0V	0.25	-	-	
CE-DI Time	1/1 duty	t_1	V_{DD}=5.0V, at CE rising	1.0	-	-	
	1/2 duty	t_{11}	V_{DD}=5.0V, at CE rising				
		t_{12}	V_{DD}=5.0V, at DI falling				
CE-CK Time	1/1 duty	t_2	V_{DD}=5.0V, at CK rising	1.25	-	-	
	1/2 duty	t_{21}	V_{DD}=5.0V, at CK rising				
		t_{22}	V_{DD}=5.0V, at CK rising				
CE Disable Time	1/2 duty	t_3	V_{DD}=5.0V, at CE falling	4.0	-	-	

TIMING CHARACTERISTICS

-. 1/1 duty(56 bits)



-. 1/2 duty(112 bits)

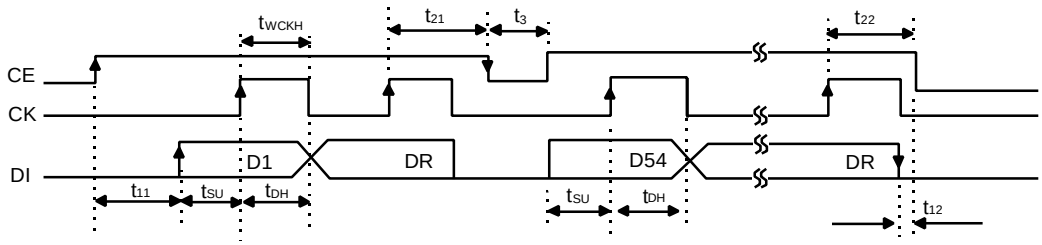
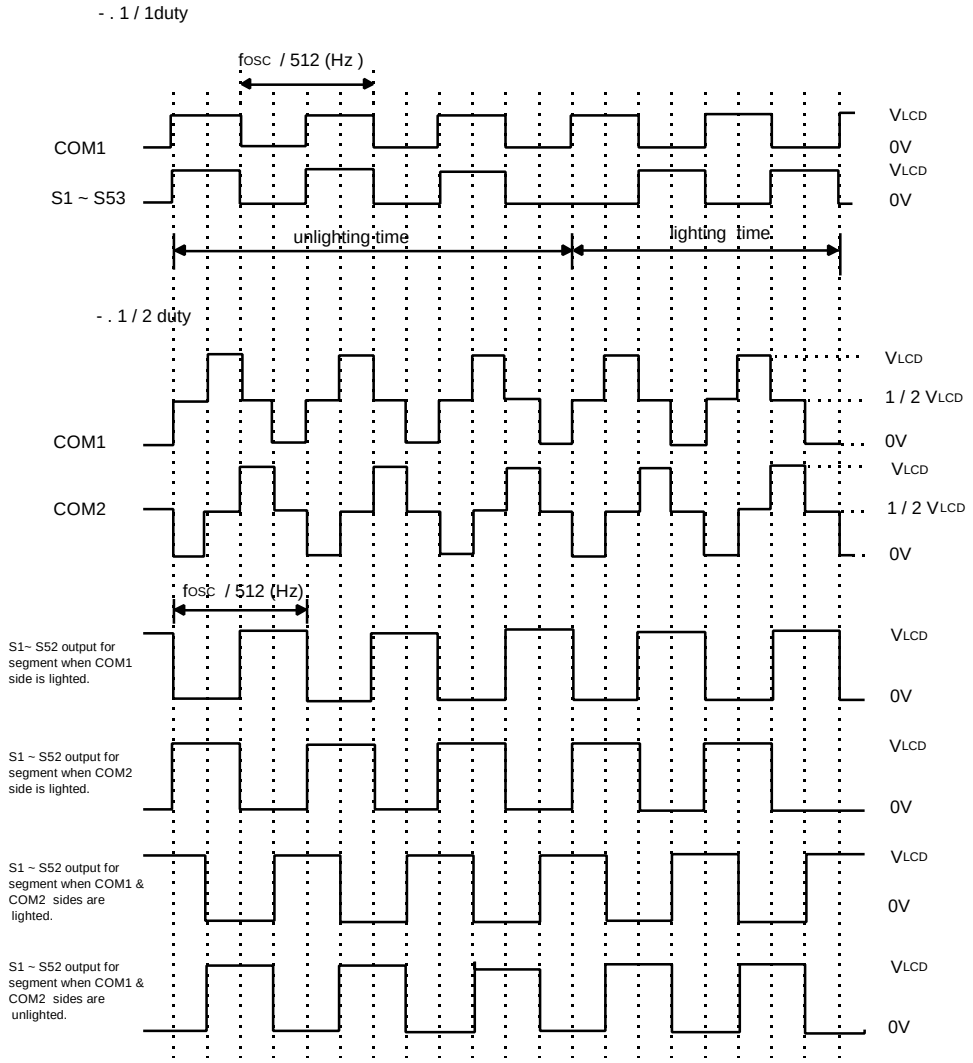


Fig. 1. AC Characteristics

OUTPUT WAVEFORM



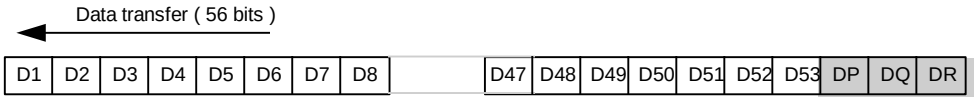
BLOCK FUNCTION

CLOCK GENERATOR

The oscillator is operated by connecting external resistor and capacitor.
The clock of oscillator block is used as signal of common
and segment driver.

FUNCTION DECODER

Function decoder generates, using chip enable (CE), data (DI),
clock (CK) from controller, a signal which controls the function
and mode of chip. for example AD / DSP function , drive mode, latch
clock select and so forth.



DP : Drive mode select bit →1 / 1 duty at " 0" , 1 / 2 duty at " 1"
DQ : AD / DSP function select bit → Segment output at " 0 ". AD / DSP function at " 1 "
DR : Latch clock select bit → latch1 clock at " 0 " , latch 2 clock at " 1 "

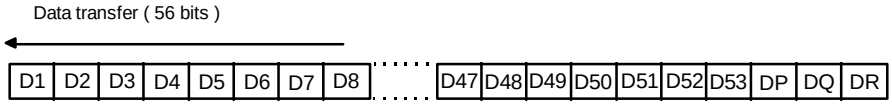
NOTE) If AD / DSP function selected are not in use, ARI, ALI, DSP1, DSP2 pins are connected to VDD or VSS
in order to protect floating.

SHIFT REGISTER

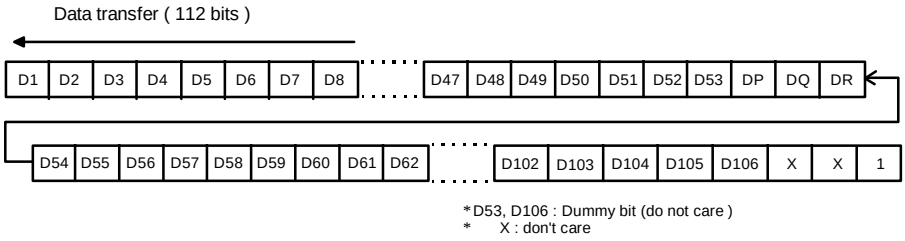
Shift register consists of 53 data bits for display and 3 bits for function / mode select.

Data transfer mode

. 1 / 1 duty



. 1 / 2 duty

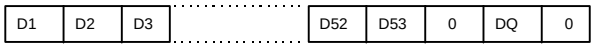


- . D1 ~ D53 : Display data (1 / 1 duty) → lighted at " 1 "
- . D1 ~ D106 : Display data (1 / 2 duty) → Unlighted at " 0 "

NOTE) If AD / DSP functions are selected
- . 1 / 1 duty : D46 ~ D53 → Dummy bit (don 't care)
- . 1 / 2 duty : D88 ~ D106 → Dummy bit (don 't care)

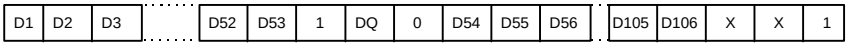
The example of data transfer

. 1 / 1 Duty

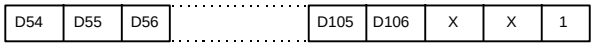


.Under 52 segments at 1 / 2 duty

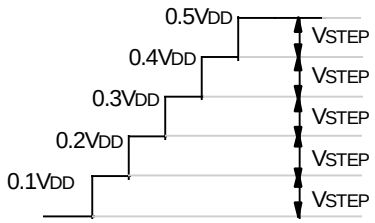
.Over 52 segments at 1 / 2 duty



.Under 52 segments at 1 / 2 duty , Data can not be transferred as below figure.



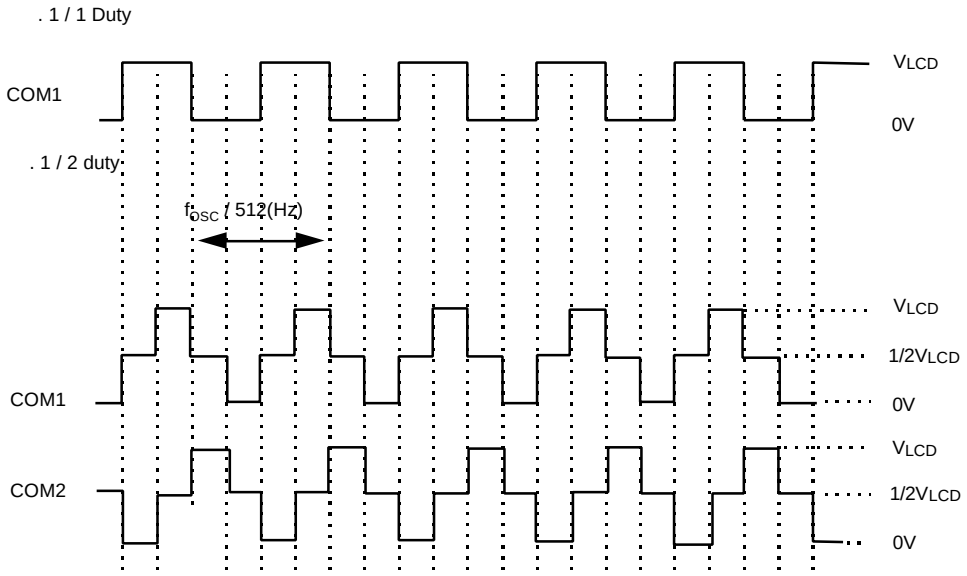
ADC (ANALOG TO DIGITAL CONVERTER)



ADC consists of two analog inputs (ARI , ALI) and two ADCs for level meter, and converts a analog input to 5 - level digital data in order to drive level meter.

Fig. 2. Step voltage difference input voltage on S45 (ALI) , S47(ARI)

COMMON DRIVER



LATCH AND SEGMENT DRIVER

. Latch has two signal, latch 1 clock latches D1 to D52 in 1/1 duty mode or 1/2 duty mode.
latch 2 clock latches D54 to D105 in 1 / 2 duty mode
D53 and D106 mean dummy bits (Don¡t care) at 1 / 2 duty mode
. If AD / DSP function is selected, S44 to S47 are input pins, S48 to S53 are output pins.

CORRESPONDENCE BETWEEN TRANSFER (EXTERNAL INPUT) DATA AND OUTPUT PIN

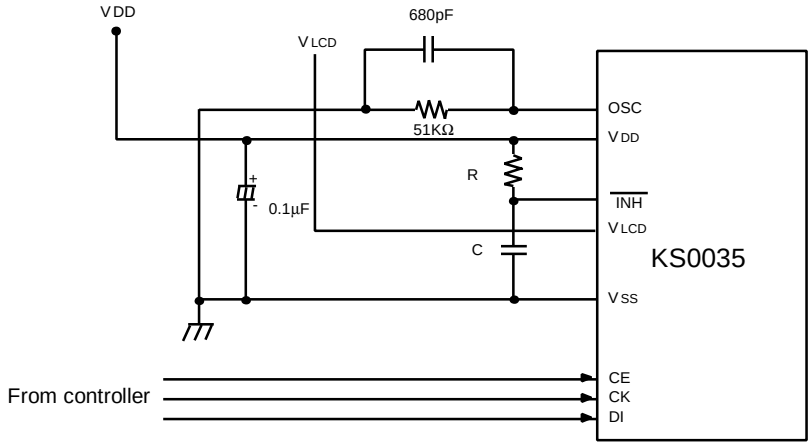
NOTE : In the case of 1 / 1duty, only COM1 is used.

DP / DQ / OUTPUT	0		1		COM1	COM2
	0	1	0	1		
	1/1 duty		1/2 duty			
S1	D1	D1	D1	D1	¡	
			D2	D2		¡
S2	D2	D2	D3	D3	¡	
			D4	D4		¡
S3	D3	D3	D5	D5	¡	
			D6	D6		¡
.	.	.	.	.	.	.
S26	D26	D26	D51	D51	¡	
			D52	D52		¡
S27	D27	D27	D54	D54	¡	
			D55	D55		¡
S28	D28	D28	D56	D56	¡	
			D57	D57		¡
.	.	.	.	.	.	.
S43	D43	D43	D86	D86	¡	
			D87	D87		¡
S44	D44	D44	D88	*DSP2	¡	
			D89			¡
S45	D45	D45	D90	*ALI	¡	
			D91			¡
S46	D46	*DSP1	D92	*DSP1	¡	
			D93			¡
S47	D47	*ARI	D94	*ARI	¡	
			D95			¡
S48	D48	*DSPO1	D96	*DSPO1	¡	
			D97	*DSPO2		¡
S49	D49	*ARO1	D98	*ARO1	¡	
			D99	*ALO1		¡
S50	D50	*ARO2	D100	*ARO2	¡	
			D101	*ALO2		¡
S51	D51	*ARO3	D102	*ARO3	¡	
			D103	*ALO3		¡
S52	D52	*ARO4	D104	*ARO4	¡	
			D105	*ALO4		¡
S53	D53	*ARO5	ALWAYS LIGHTING	*ARO5	¡	
			ALWAYS LIGHTING	*ALO5		¡

*NOTE : DSP1, DSP2 : External display input data
DSPO1, DSPO2 : External display output data
ARI , ALI : AD converter input data
ARO1 to 5, ALO1 to 5 : AD converter output data.

APPLICATION CIRCUIT

Application circuit 1



Application circuit 2